AN INTEGRATED VOICE/DATA LOCAL AREA NETWORK

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by

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CERTIFICATE

Certified that this work 'AN INTEGRATED VOICE/ DATA LOCAL AREA NETWORK' by Capt. K. Kamesh has been carried out under my supervision and has not been submitted elsewhere for a degree.

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ABSTRACT

A demand assigned distributed control Time Division Multiple Access (TDMA) point-to-point store-and-forward loop network suitable for voice/data integration in a local area environment is discussed. A review of the current state-of-art in switching, network topologies and multiaccess techniques is carried out. Special emphasis has been placed on the study of the suitability of fast circuit switching vis-a-vis packet switching. The need to adhere to the dictates of voice, being the major source of traffic, has been stressed. The fast circuit switched approach was selected for reasons cited therein.

Based on traffic statistics the network is evolved for a 1000 user environment. The network is based on subscriber access to a 64 Kbps slot employing 'in-slot' signalling. The front-end-processor for a node for a scaled-down prototype employing a 16 slot/frame format has been implemented. The design is modular, permitting implementation of all nodes on identical lines. The design minimises hardware/software requirements for further processing.

The network uses a fast circuit switched approach (small call set up and relinquish times) and provides high throughput. The expected performance analysis is carried out in terms of call set up and relinquish times and capacity utilisation.

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CHAPTER 1

INTRODUCTION

Historically communication networks have evolved keeping in mind the needs of telephony. Low speed data traffic such as telegraphy, teleprinter and teletype were conveniently accomodated within the bandwidth (BW) of a voice channel. FDM techniques were used for this purpose. With the advent of computers the data processing power has increased manifold. As a consequence the data traffic is increasing. Separate networks (NW) were evolved to meet the local requirements. Subsequently, the need for a single network (NW) which can provide customer access to all kinds of services was felt and the concept of an Integrated Services Digital Network (ISDN) was evolved. Such a concept had to be centred around the needs of telephony for it still remains the single largest source of traffic to a communication carrier.

In this thesis the design and implementation of an ISDN suited for a local area environment using a fibre - optic or other point to point data links has been attempted. The network is based on a demand assigned distributed control Time Division Multiple Access (TDMA) where each TDMA slot is compatible for PCM voice traffic.

1.1 INTEGRATED SERVICES DIGITAL NETWORK (ISDN):

An analysis of the relative importance of telecommunication services in 1979 (Table 1.1) [1] shows that more than 90% of the traffic is still due to voice. However the analog network suffers from two limitations - speed and large call set up times. Table 1.2 shows the speed limitation of the analog network. Table 1.3 gives a performance comparison of the network in relation to non voice services. The concept of the ISDN had to be evolved based on these three aspects.

Table 1.1: Relative Importance of Telecommunication Services in 1979 [1].

Service	Country					
	Belgium	France	Germany	Italy	Spain	UK
Telephone	2300	14000	19200	13400	10500	25000
Telex	19	85	130	44	21	100
Low speed data on telephone network	3	20	95	18	3	150
Leased lines	6	40	NA	56	12	250
Packet switched data	-	1	trial	trial	8	trial
Circuit switched data	-	2	3	3	-	-

Note: 1. Figures refer to the numbers of subscribers in thousands
2. NA - not available

Table 1.2: Speed Limitation of Analog Networks [1]

Service	Bit rate on analog network (kbit s^{-1})	Transmission time for one page (seconds)	Desirable transmission time (seconds)	Required bit rate (kbit s^{-1})
Videotex	1.2	10	1	9.6
Teletex	2.4	10	2	9.6
Facsimile Group 3	2.4	120	5	64

Table 1.3: Performance Comparison of Network in Relation to non-voice services [1].

Parameter	Public switched telephone network (analog)	Private network	Public switched data network	ISDN objective (tentative)
Call duration	120 s	leased path	circuit: 10 to 3600 s packet: 10 ms to 1 s	variable mix
Call setup time	3 to 20 s	NA	circuit: 0.1 to 1 s packet: 1 to 10 s	1 to 3 s
Information transfer time	10 s	10 s	circuit: 10 ms packet: 0.1 to 1 s	10 ms
Error ratio	10^{-4}	10^{-6}	circuit: 10^{-6} packet: 10^{-10}	10^{-6}
Bit rate	2.4 kbit s^{-1}	any	upto 48 kbit s^{-1}	upto 64 kbit s^{-1}

Note: 1. N/A - not applicable

The CCITT defines an ISDN as 'An integrated digital network in which the same digital switches and the same digital paths are used to establish connections for different services, e.g. telephony and data'. Further CCITT has stated that the ISDN will evolve from the basis of a digital telephone network with integrated switching and transmission by the addition of new non-voice services, by providing access to dedicated networks and eventually by providing all services over a common network. Table 1.4 lists some candidate services for integration. A major factor in this evolution is the provision of digital subscriber access based on a 64 Kbps main channel and an out-slot (i.e. out side 64 Kbps) signalling channel.

Table 1.4: Candidate Services for Integration [1]

Bandwidth	Service			
	Telephony	Data	Text	Image
Digital voice (64 kbit s^{-1})	Telephone	Packet switched data	Telex	
		Circuit switched data	Teletex	
	Leased circuits	Leased circuits	Leased circuits	
	Information retrieval (by voice analysis and synthesis)	Telemetry	Videotex	
		Funds transfer	Facsimile	
		Information retrieval	Information retrieval	Information retrieval
		Mailbox	Mailbox	Surveillance
		Electronic mail	Electronic mail	
		Alarms		
Wide-band (>64Kbit s^{-1})	Music	High speed computer communication		TV conferencing videophone, Cable TV distribution

1.2 LOCAL AREA NETWORKS:

Local area networks (LAN) offer another approach to the integration problem. These networks generally are a few kilometers in diameter with data rates exceeding 1 Mbps. These, too, are capable of providing the subscriber services needed. Local area computer network (LACN) is a variation of the above. Custom built networks of various kinds are also available. All these networks in general use digital switching techniques for processing a digital data stream. 64 Kbps PCM (defined as one traffic channel (TC)) has been generally accepted as the standard technique for digitising voice [2]. However, no international specifications are yet available in this area.

1.3 OUTLINE OF THE THESIS:

Chapter 2 reviews the switching techniques, network topologies and multiaccess techniques. Based on the various aspects discussed in Chapter 2, Chapter 3 proceeds to design a network suitable for integration of various kinds of services in a local area environment. Chapters 4 and 5 discuss the hardware aspects of one unit of the network - the front-end processor of a node. The former devotes itself to the timing recovery problem while the latter discusses Input/Output processing of data. The expected performance

of the network in terms of call set up and disconnect times and capacity utilisation is discussed in Chapter 6. The thesis concludes with Chapter 7 containing a few suggestions for future work.

CHAPTER 2

OVERVIEW

This chapter presents a brief review of the options available while designing a network in terms of switching, topology and access technique. The various parameters of interest - call set up and disconnect times, delay, effective circuit utilisation time, cost, throughput etc. - are discussed in brief.

2.1 SWITCHING:

A call between two subscribers requires that

i) A permanent path exists between them for all times - leased lines.

ii) A path exists between them for the duration of the call - circuit switching.

iii) No path is held between subscribers but the information is switched from end to end-message / packet switching.

2.1.1 Circuit Switching:

There are two ways in which a path between two subscribers can be established:

i) A physical (copper) path is switched to establish a circuit.

ii) A virtual path is established for the duration of the call-virtual circuit switching.

2.1.2 Circuit Switching Options:

a) Traditional circuit switching:

A switch sets up a dedicated connection between subscribers for the full duration of use. This has the advantage that the subscribers can carry on a conversation or transact data unaffected by the loading of the network. The data rate or bandwidth is, however, limited only by the bandwidth assigned to the user. The main disadvantage is that call set up times are fairly large and increase with the loading of the network.(Fig. 2.1) [3].

b) Fast circuit switching:

This, like traditional circuit switching, uses signalling messages to set up and disconnect a path. The signalling speed, however, is very great. This is of great use when interactive data users are considered. The idle circuit capacity during the 'think' time of an interactive data user could be used to transfer data from other users, thus increasing the efficiency of the network. Public networks are aiming at a call set up/disconnection delay of 140 ms over long distances using advanced digital switches. This

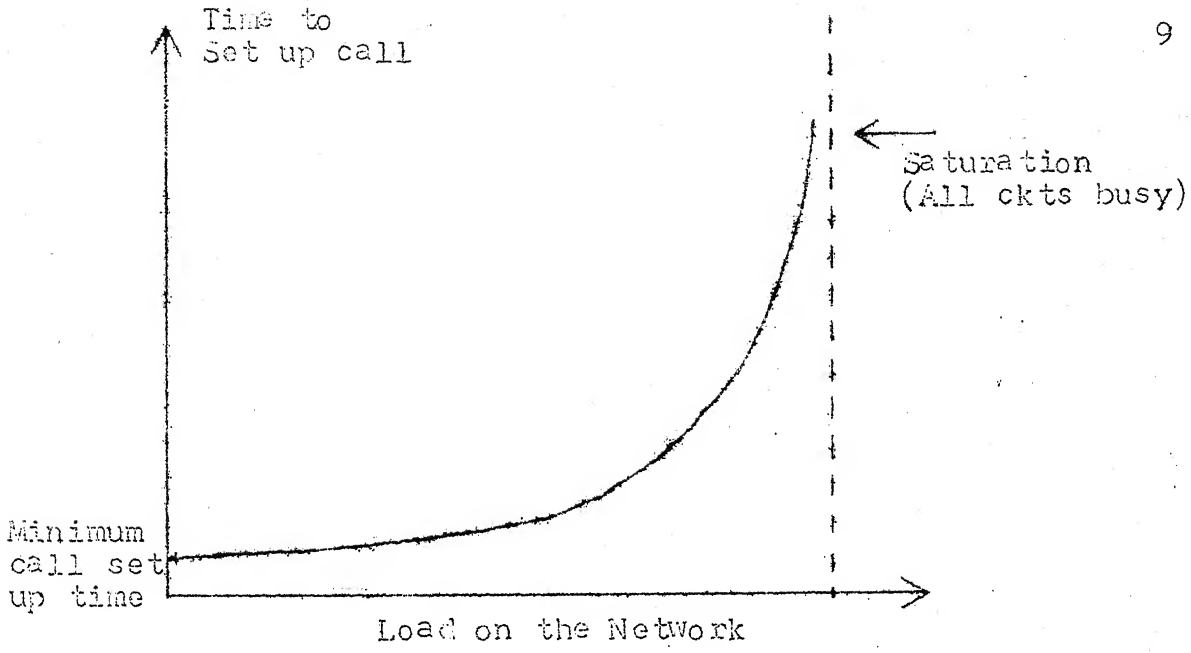


Fig. 2.1(a): Connection delay versus load on the Network [3]

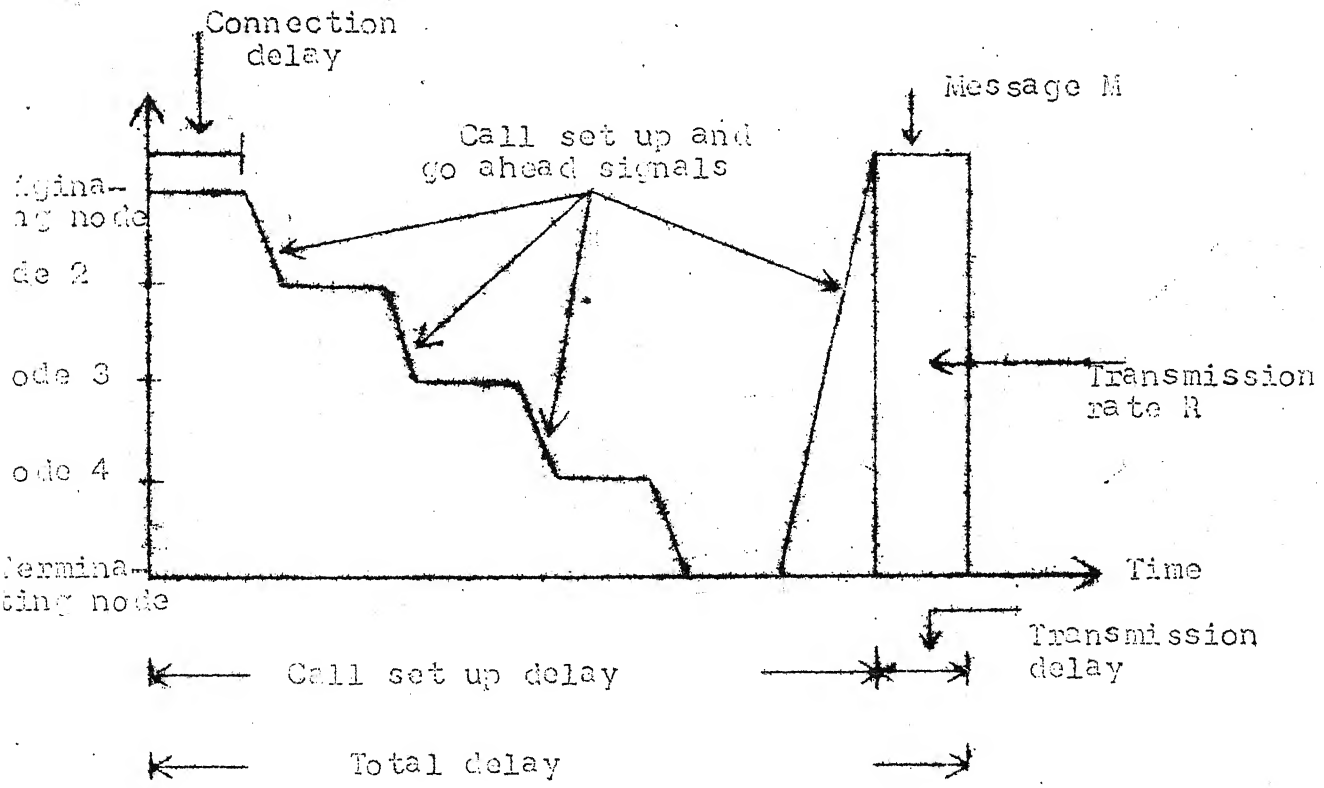


Fig. 2.1(b): Total network delay components [3].

would satisfy the strict end to end delay requirements of 200 or 250 ms for interactive data applications [3].

c) Enhanced circuit switching:

This method is a design concept that attempts to over come the poor transmission efficiency associated with traditional circuit switching of voice and interactive data by using traditional circuit switching supplemented with Time Assigned Speech Interpolation (TASI) for voice and demand adaptive multiplexing for interactive data. TASI makes use of the fact that speech is actively present on a busy channel for about 40% of the time. The low activity is largely due to the fact that a subscriber speaks less than half the time during a conversation and that each subscriber's speech is carried on a separate channel. This was originally used on submarine cables. A variation of this technique called Digital Speech Interpolation (DSI) has been used for TDM systems. Good performance has been obtained using DSI over satellite channels [4-5]. The mathematical analysis of data performance in a system where data packets are transmitted during voice silent periods for a single channel case has been carried out by Fischer [6]. Fig. 2.2 shows the comparison of data performance for a voice load of 0.1 Erlangs. The results seem to indicate that

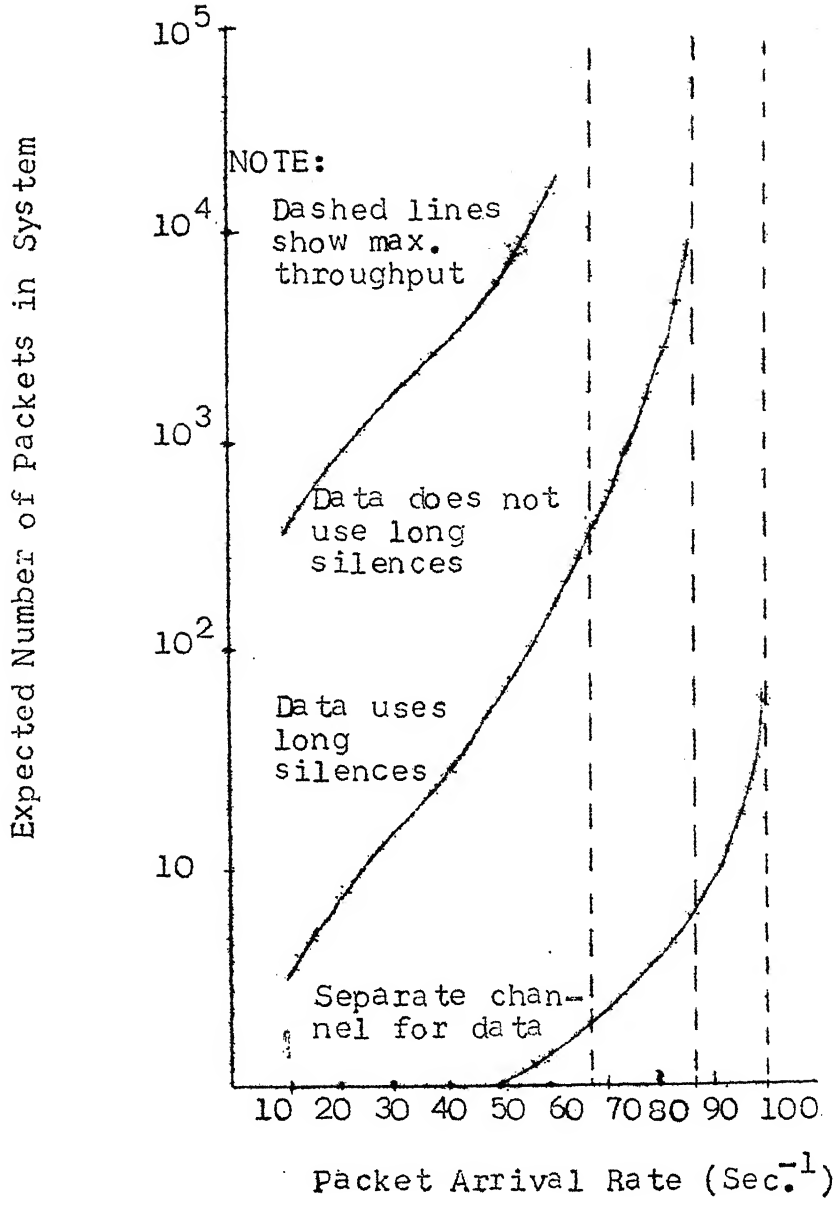


Fig. 2.2: Comparison of Data Performance for Voice Load of 0.5 Erlang [6].

i) the expected number of data packets is significantly reduced when one allows data to be transmitted during long silences only.

ii) Maximum throughput increases as the voice load is increased.

2.1.3 Packet Switching:

Data traffic is characterised by fairly short messages exchanged at high speeds. This characteristic is made use of in packet switching. A block of data is transmitted from node to node. The block of data may be stored and transmitted or transmission may commence before the data has arrived completely (called virtual cut through). Packet switching is often regarded as a particular form of message switching. The major differences between the two are:

a) Messages are moderately unrestricted in size compared to packets.

b) Messages usually have a format depending on certain markers or codes while packets generally have a fixed format.

c) Message switching emphasizes the responsibility of the NW for correct transmission of the message.

Experiments have been carried out for transmitting voice over a packet-switched network [7-11]. There are several difficulties associated with this form of transmission of voice. For example the interarrival times of packets vary. This could lead to severe problems in reconstruction,

and distortion of speech. Packets could arrive out of sequence but this could be taken care of by a sequencer. Lost packets constitute another major problem for repetition requests and repetitions require time. Further packet switched voice would require high throughput and low delays. These problems could, perhaps, be overcome by special flow control measures and speech encoding to reduce data rates. There seems to be a general concurrence that while voice is best transmitted by a circuit-switched approach, data is best transmitted by a packet-switched approach. A hybrid system called Transparent message switching [8] employing circuit switched approach for voice and packet switched approach for data is emerging. The movable boundary frame format seems to provide good results[12]. The fixed frame boundary format with varying proportions of speech and data was also studied. These, too, seem to be suitable for the present case viz., integration of voice and data.

2.2 CONCENTRATION VERSUS MULTIPLEXING:

The node can accept information from the subscribers and output it to the next node in some pre-assigned technique. This is called multiplexing. In this case the channel capacity $\geq \sum^{is}$ greater than or equal to the sum of the individual node bit rates. This arrangement is unsatisfactory. The

node load pattern varies with time and effective utilisation of the channel capacity cannot be achieved. One solution is to use a channel with less capacity than the sum of input lines. This is called concentration. This would need a dynamic assignment technique for the slots. A comparison between fixed and dynamic channel allocation is shown in Table 2.1. Yet another solution is to transmit two characters for each input character - the subscriber number and data.Concentrator using this principle are often referred to as statistical multiplexers or Asynchronous Time Division. multiplexers (ATDM) [13].

2.3 TOPOLOGY OF THE NETWORK:

The earliest network evolved in communications was the star, as used in the local telephone exchanges even today. Inter-exchange networks have been of the mesh or tree type. Other topologies preferred in LAN and LACN are the ring and the bus. A comparison of the star,ring and tree in terms of different characteristics is shown in Table 2.2. Fig. 2.3 shows the schematic of the various topologies.

The choice of a particular topology affects the routing algorithms. For example in a unidirectional loop there is no need for a routing algorithm while they are very important for a mesh and star type architectures.

Table 2.1: Comparison between fixed and dynamic channel allocation [2].

Characteristic	Fixed channel allocation	Dynamic allocation
Dependence of signalling and data services	Independent	Dependent
Capacity for signalling	High but limited	Allocated as required
Capacity for additional data services	Reduced	Enhanced
Usage of the total channel capacity	Lower	Higher by message interleaving
Adaptation for data service protocols	Not required	May require additional or modified protocols
Circuit realization		
- Circuit costs	Lower	Higher (VLSI and standardization would reduce costs)
- Equipment modularity	Good(information types clearly separated)	Poor(mixed information type).
- Reliability and testability	Good	Dependent on technology Poor (more complex equipment).
Flexibility	Low	High

Table 2.2: Comparison of star ring and tree topologies [14].

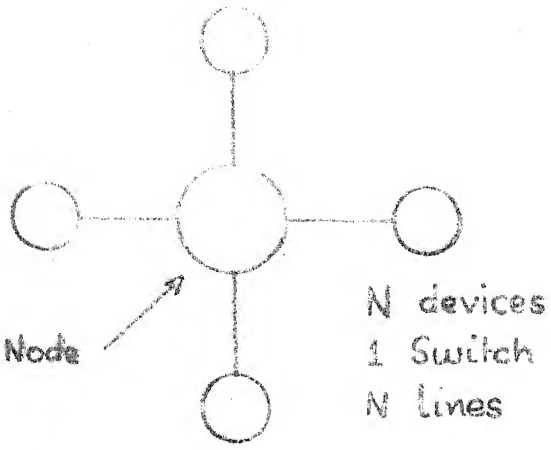
Property	Star	Ring	Tree
Length of cable	Maximum R	Minimum 2R	In between
Security	Good	Poor	Poor
Loop continuity for other nodes if one link fails	Relatively independent	If one link fails the whole system fails.	If trunk links fail a number of nodes may be cut off.
System expansion	Flexible	Fixed to the BW of cable	Relatively flexible
Multiplexing.	Relatively little	High speed	In between
BW of cables required.	Minimum B	Maximum upto nB	A mix of cables of different BW upto nB
Flexibility of service offerings	Limited by BW	Instantaneous BW is much larger	Limited by bandwidth (BW)
Switching	Central	Distributed	Distributed

Legend:

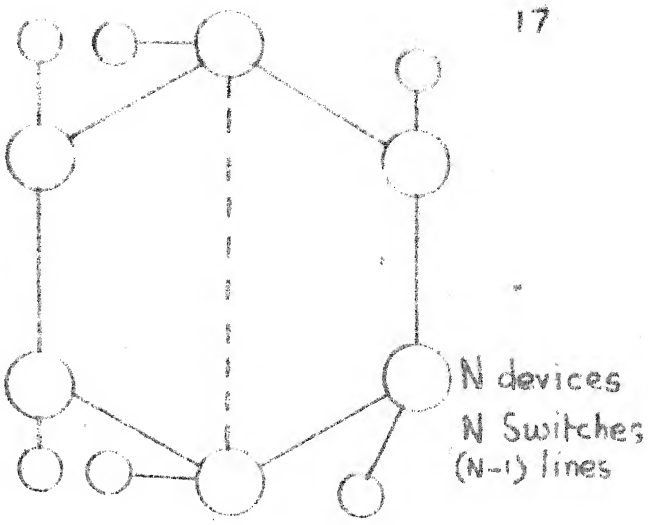
n - no. of users

B - Bandwidth (BW) per user

R - Distance between node and user.

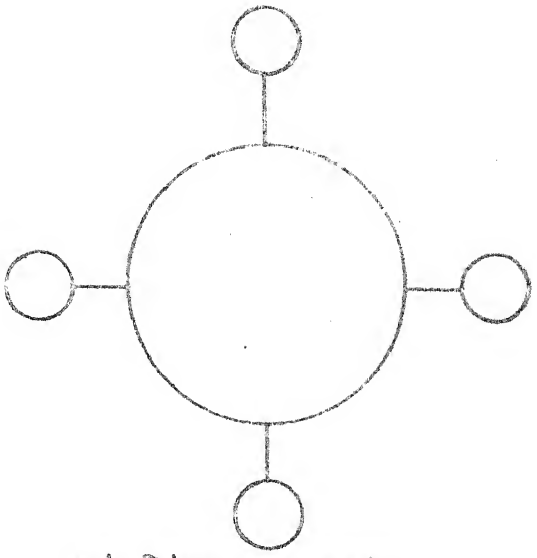


(a) Star network

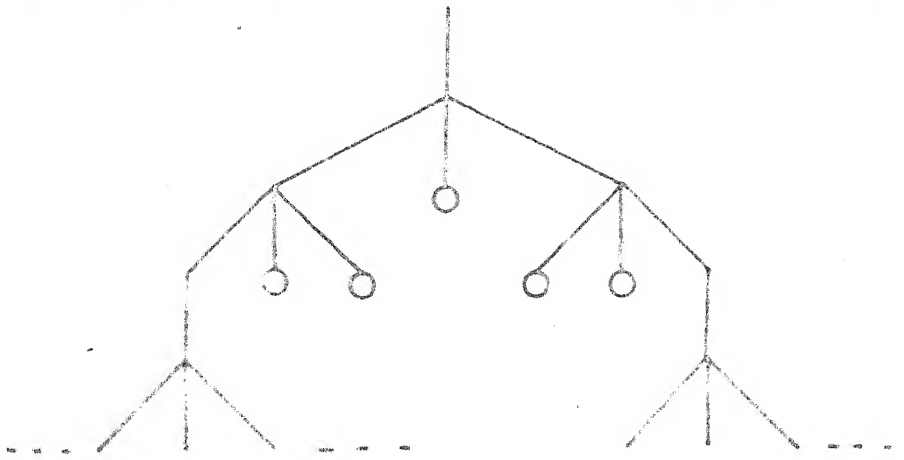


(b) Mesh Network

(c) Bus network



(d) Ring network



(e) Tree network

Fig. 2.8: Schematic of Various Topologies

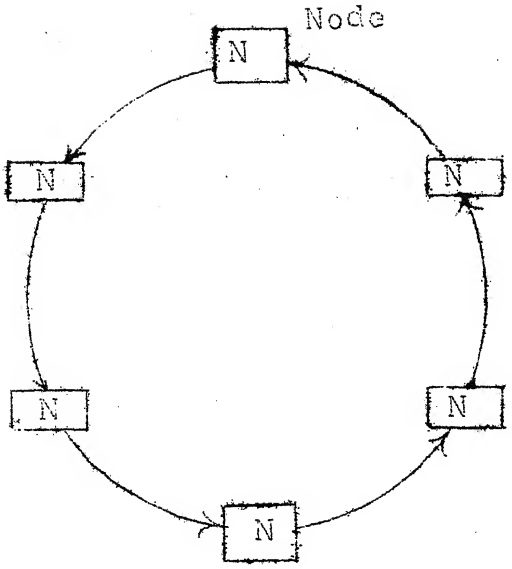
Network costs is another major governing factor which overides a number of considerations. Generally 40% of the cost of the network lies in the cost of the cable. Thus a loop/ring becomes a natural choice from the point of view of cost. However a loop is likely to fail with the failure of any one link. Duplicating every link is a poor solution. A better method (shown in Fig. 2.4) would be to bypass the defective node.

2.4 MULTI-ACCESS TECHNIQUES:

Tobagi [15] classifies the various multiaccess techniques into five categories. Table 2.3 lists these techniques with examples. For local area environments the main characteristics exploited in devising multiaccess schemes are the short propogation delay and high data rates. The main performance characteristics that are desirable are high BW utilisation and low message delays. To achieve higher BW utilisation it is essential for an access technique to simultaneously support traffic of different types, different priorities and delay requirements. In addition, robustness is most desirable.

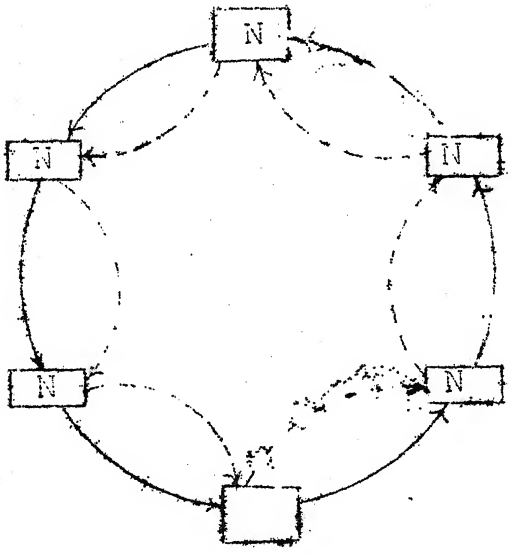
2.5 CONCLUSION:

The various switching schemes, network topologies and multiaccess techniques used in circuit switched, or,



Note: N- Node

Fig. 2.4(a): The basic loop



Note: Dotted lines indicate alternate path available

Fig. 2.4(b): Duplicating the ring

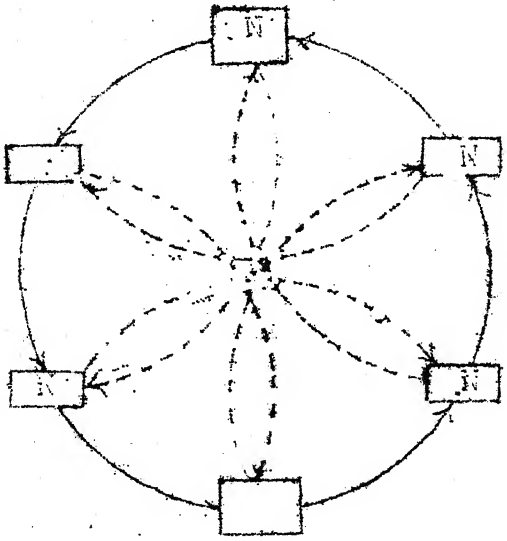


Fig. 2.4(c): Alternate method of introducing

Table 2.3: Multiaccess Techniques [15].

A. FIXED ASSIGNMENT TECHNIQUES	B. RANDOM ACCESS TECHNIQUES
1. FDMA - Frequency division multiple access	1. a. ALOHA b. Slotted ALOHA
2. TDMA - Time division multiple access	2. CSMA-carrier sense multiple access.
3. CDMA - Code division multiple access	3. SSMA - Spread spectrum multiple access
C. CENTRALLY CONTROLLED DEMAND ASSIGNMENT TECHNIQUES	**D. DEMAND ASSIGNMENT TECHNIQUE WITH DISTRIBUTED CONTROL**
1. Circuit oriented - FDMA, TDMA	1. Reservation ALOHA
2. Polling systems	2. A FIFO reservation scheme
3. Adaptive polling systems	3. A Round Robin reservation scheme
4. SRMA- Split channel reservation multiple access	4. Mini-slotted alternating priorities (MSAP)
5. GSMA- Global scheduling multiple access	5. Assigned slot listen before transmission.
	6. Distributed tree retransmission algorithms
	7. Distributed control algorithms in LAN - Token passing - Pierce loop - Register insertion

E. ADAPTIVE STRATEGIES AND MIXED NODE

1. The URN scheme
2. Another Adaptive strategy
3. Reservation upon collision
4. PODA - Priority oriented demand assignment
5. Mixed mode -
   - MACS - Mixed Aloha Carrier Sense
   - GRA - Group Random Access

packet switched networks have been briefly reviewed. Certain engineering considerations concerning the choice of topology, cost and other parameters of the network have been brought out.

CHAPTER 3

DESIGN OF A LOCAL AREA ISDN

The previous chapter summarises the network topologies, protocols and switching techniques. The evolution of a network architecture suitable for supporting an integrated voice-data traffic in a local area environment is discussed.

3.1 AIM:

To design a digital LAN which

- is capable of providing duplex voice/data communication between subscribers
- is suitable for interactive data users
- is capable of transferring bulk data, if required
- may utilise large data rates
- provides maximum throughput

3.2 SYSTEM DESIGN:

As per CCITT specifications the provision of digital subscriber access based on a 64 Kbps channel is important for an integrated voice/data network. It was pointed out in Chapter 2 that the virtual circuit switched approach is best suited for voice. One consequence of the above assumptions is that the TDMA n slots per frame format which

can support a variable mix of voice and data is indicated. This structure is adopted in this thesis.

3.2.1 Choice of Frame Repetition Rate:

In order to transmit voice it is necessary to transmit 8000 samples/sec. with a resolution of 8 bits/sample (64 Kbps PCM). In order to reconstruct speech from the digital input it is necessary to receive the voice samples at the sampling rate. It is generally convenient to transmit an integral multiple of samples for it reduces hardware/ software problems during reconstruction. Thus frame rate $F = 8000/n$ where F and n are integers. If n is small the word is small. This leads to lower throughput. A large value of n leads to a long word which becomes unwieldy. Thus transmitting 4 samples per frame seems to be suitable. This leads to a word length of 32 bits and a frame rate of 2000/sec. Further a 32 bit slot appears to be well suited for the transmission of 4 bit DPCM, 8 bit PCM and 2x16 bit PCM and for reducing high bit rates by serial to parallel conversion on a bus [17].

3.2.2 Choice of Number of Slots/Frame:

All users connected to a network are not active at all times. A single device occupied continuously or intermittently for a total time t during a period T,

carries, by definition, t/T Erlangs of traffic. A typical figure for maximum (busy hour) traffic flow in the telephone system is 0.1 Erlangs/subscriber [16]. Assuming calls to be in accordance with a stationary Poisson distribution we can apply Erlang's lost call formula which states that

$$E_{1,n}(A) = \frac{A^N}{N} / \left(1 + \frac{A}{\lfloor 1} + \frac{A^2}{\lfloor 2} + \cdots \frac{A^N}{\lfloor N}\right)$$

or

$$E_{1,n}(A) = \frac{A^N}{N} / e^A \text{ for large } N$$

where,

$E_{1,n}(A)$ is the call blocking probability

N is the number of time slots or virtual circuits

A is the traffic offered by all sources in Erlangs (A=0.1xM)

M is the number of sources.

Assuming a call blocking probability of .001 (i.e. 1 out of 1000 calls are lost) the number of circuits/slots required is approximately 74. In addition the following information needs to be transmitted -

a) Frame synchronisation signal

b) Status information of the node

c) Some error correction/detection information such as CRC check sum.

It is seen that a 100 slot/frame,2000 frames/second format adequately meets the needs of a 1000 user environment.

3.2.3 Slot Header:

The offered traffic varies from node to node. It also varies with time. Thus a fixed assignment of slots to nodes would not be efficient. A centralised control of demand assignment would require additional traffic to and from the controller from each node. This would also reduce throughput. Further additional hardware/software would be required to assign / deassign slots based on requests. A collision detection scheme combined with an arbitration mechanism would reduce throughput. Distributed control is another alternative. In order to assist the node in processing a slot, some information regarding the slot would be necessary. It would also be necessary to delay the data stream by a fixed quantity to process the header information. In respect of the former the under mentioned information would be adequate

a) Slot is busy - is actually carrying traffic

b) Slot is free - Can be put to use

c) Slot carries signalling information

- concerned node has to process it

Further it may be necessary to know, say for error control coding purposes whether the slot carries voice or data. Thus a two bit header is adequate for this purpose. Since the chances of an error in the header information can not be ruled out it is necessary to transmit some kind of error check on the header information. A simple parity check seems to meet this purpose. The delay needed in the node is a measure of the processing speed. A two slot delay seems to be adequate for a simple dedicated logic to perform the necessary operations. Table 3.1 indicates the header pattern and its interpretation. Bit 4 has been included which could be used for slow speed communication or for special purposes (see Chapter 6).

Table 3.1: Slot header information

Bit 3	Bit 2	Bit 1	Bit 0	Interpretation
X	0	0	0	Slot free
X	1	0	1	Slot busy. Contains voice
X	1	1	0	Slot busy. Contains data
X	0	1	1	Slot busy. Contains signalling format

Legend

'1' - Logical high

'0' - Logical low

'X' -'Dont care' state

Bit 2 is the parity check on bits 0 and 1

3.2.4 Data Rate Calculations:

Length of slot = Length of data + length of header

= 32 + 4 = 36

No. of slots/frame = 100

No. of bits/frame = 100x36 = 3600

No. of frames/sec = 2000

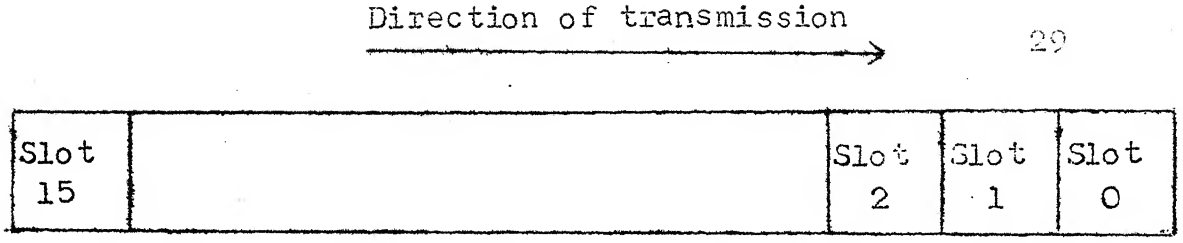
Base band channel data rate = 3.6 K x 2K = 7.2 Mbps

3.2.5 Frame Format:

Frame format is shown in Fig. 3.1. For sake of convenience it is assumed that the frame sync. information is transmitted with every frame. The various formats are discussed below.

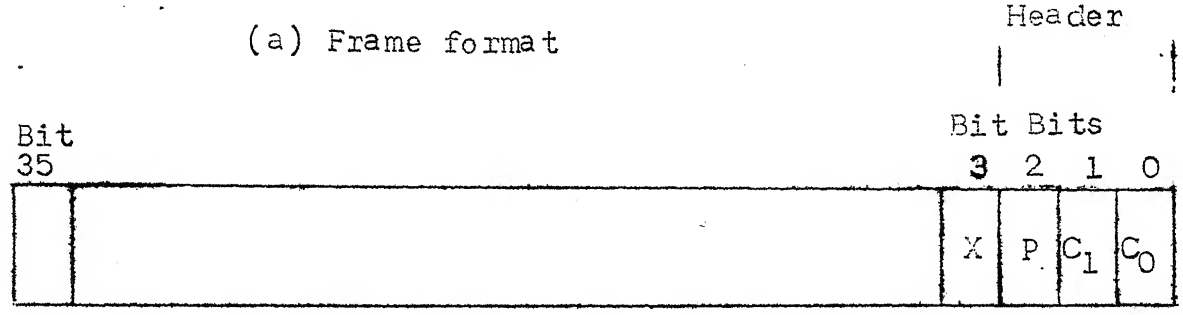
a) Frame sync. format:

The frame synchronisation word should have a unique pattern. The Ethernet for example uses a 64 bit preamble with a series of alternating band 0s the last two bits being 1. Matt [17] uses a 31 bit pseudo noise sequence while a 30 channel PCM system uses the 10011011 pattern in alternate frames [18]. The format of the synchronisation word is shown in Fig. 3.1(c). It is easily seen that the pattern is sufficiently unique.



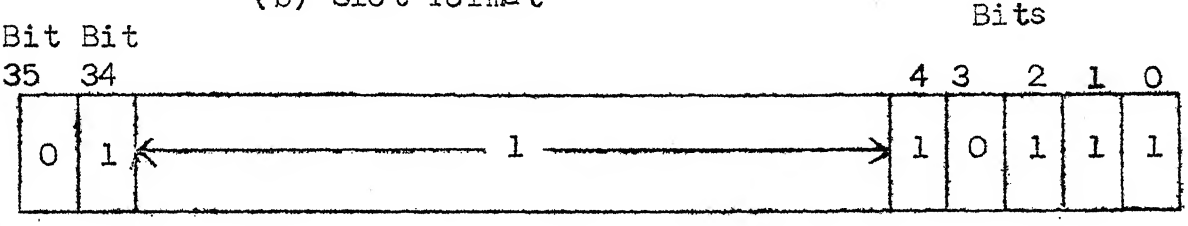
Note: Frame duration 500 μ seconds

(a) Frame format

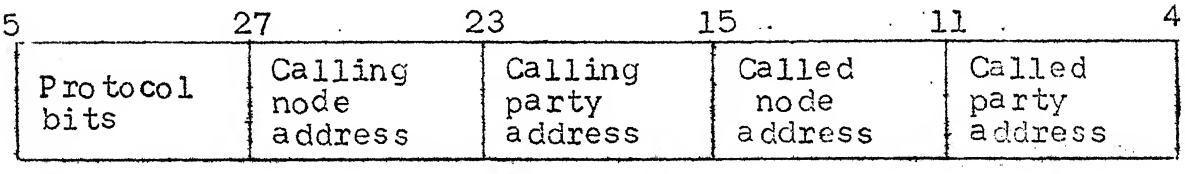


Note: Slot header information listed in Table 3.1.

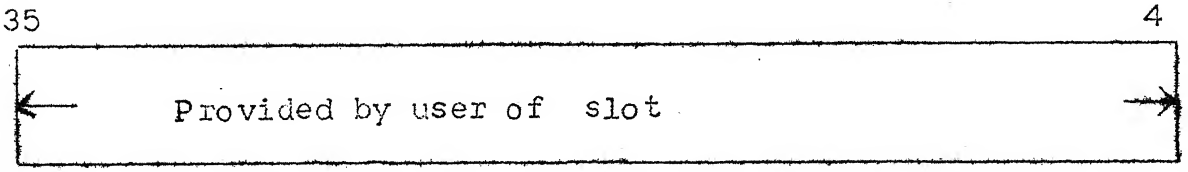
(b) Slot format



(c) Frame sync format



(d) Signalling word format



(e) Voice/data word format

Fig. 3.1: Frame Format

b) Signalling format:

Fig. 3.1(d) shows the bit assignments. This provides 4 bits/channel in the forward and reverse directions. These can be used as handshaking signals between the called and calling subscribers. For symmetry in signalling patterns the called subscriber acknowledges the call with the same pattern containing addresses in the reverse order[17].

3.2.6 Network Topology and Consequences:

It was seen in Chapter 2 that 40% of the network cost lies in the cable. It was pointed out that a loop offers the minimum cable length. A variety of measures which can be undertaken to increase reliability were also indicated. Further, a loop would obviate the need for routing algorithms. Duplex communication in the same slot would be possible. The node processor now becomes a multiplexer with the ability to assign a slot on demand by recognizing the header with each slot. Some kind of system control and interface to other networks may be necessary and this suggests a loop controller. Fig. 3.2 shows the block schematic of the network evolved.

3.2.7 Line Coding:

The binary bit stream as originated by the source is generally not suitable for transmission directly on line.

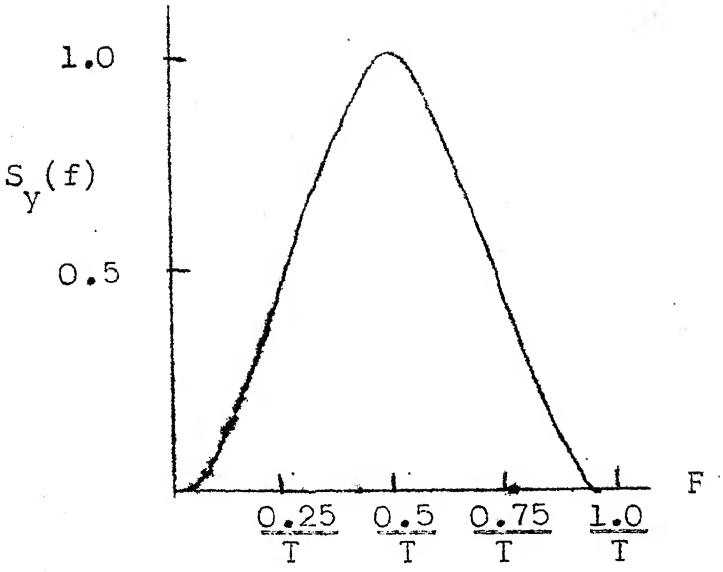


Fig. 3.2: Power spectral density of Manchester encoded signal.

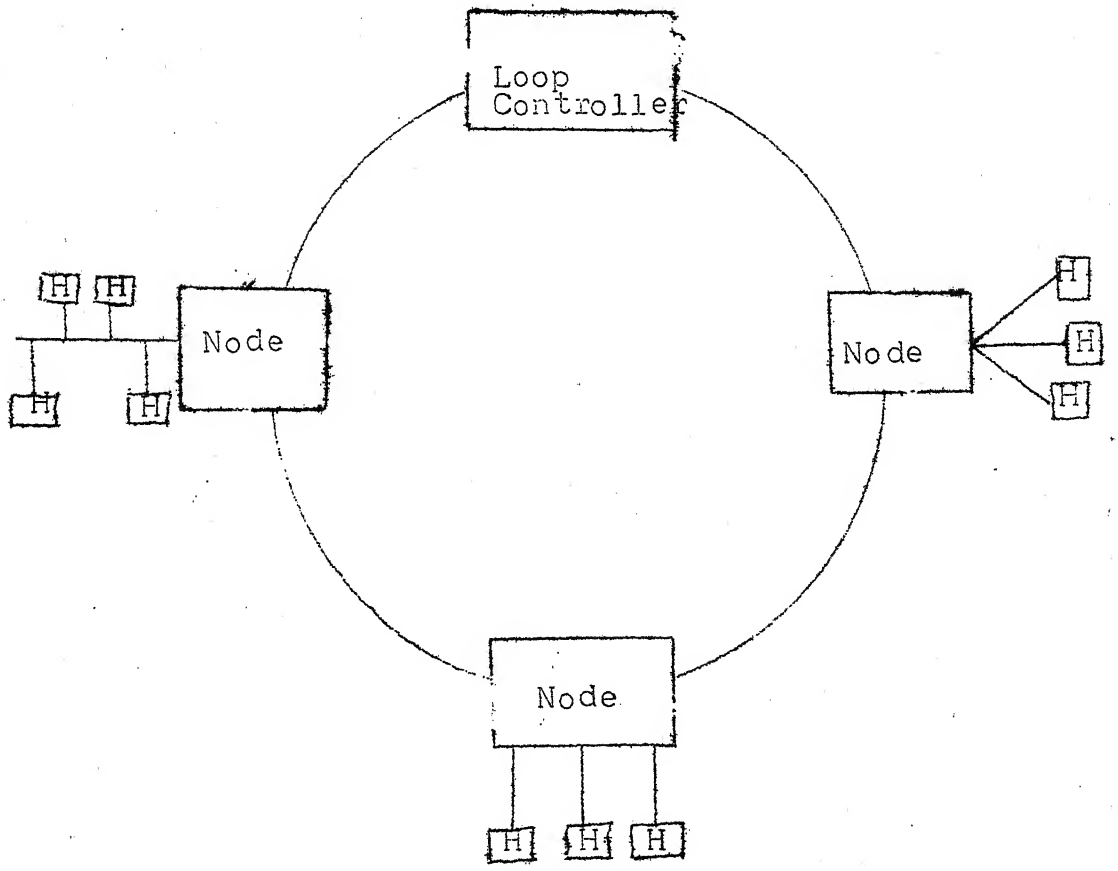


Fig. 3.3 : Block schematic: Proposed Network

Some kind of line coding such as AMI, HDB3 or Manchester coding is needed to make it suitable for transmission on line. In the present case Manchester encoding has been chosen for the following reasons:

a) It has an energy spectrum with small low frequency components and no zero frequency components (Fig. 3.2).

b) Every clock position is occupied. This assists in clock recovery

c) Monitoring of error rate of the transmitted information is possible.

d) Provides error detection capability

3.3 FUNCTIONAL DESCRIPTION:

The block schematic (Fig. 3.3) shows the three main elements of the network - the loop controller, node and channel. Some functions of the loop controller and node are described in subsequent paragraphs.

3.3.1 Loop Controller:

The loop controller is expected to perform the following functions.

i) Act as a master clock source for the entire system

ii) Transmit, receive and maintain system information.

iii) Interface the local loop to larger loops/other networks

iv) Transmit the frame sync. at the beginning of each frame.

v) Buffer the portion of the frame not in circulation.

vi) Provide space to store and retrieve information to all/selected users in the node.

vii) Provide toll information

3.3.2 Node Processor:

Fig. 3.4 shows the block schematic of the node processor. The node is expected to perform the following functions.

a) Assist in setting up a call/termination of call for the user.

b) Process the serial data stream and retransmit it.

c) Maintain synchronism

d) Recover symbol timing for use in the node

e) Recognize faults if any and provide correction.

f) Automatically bypass the node in the event of a major breakdown and inform the loop controller of the same.

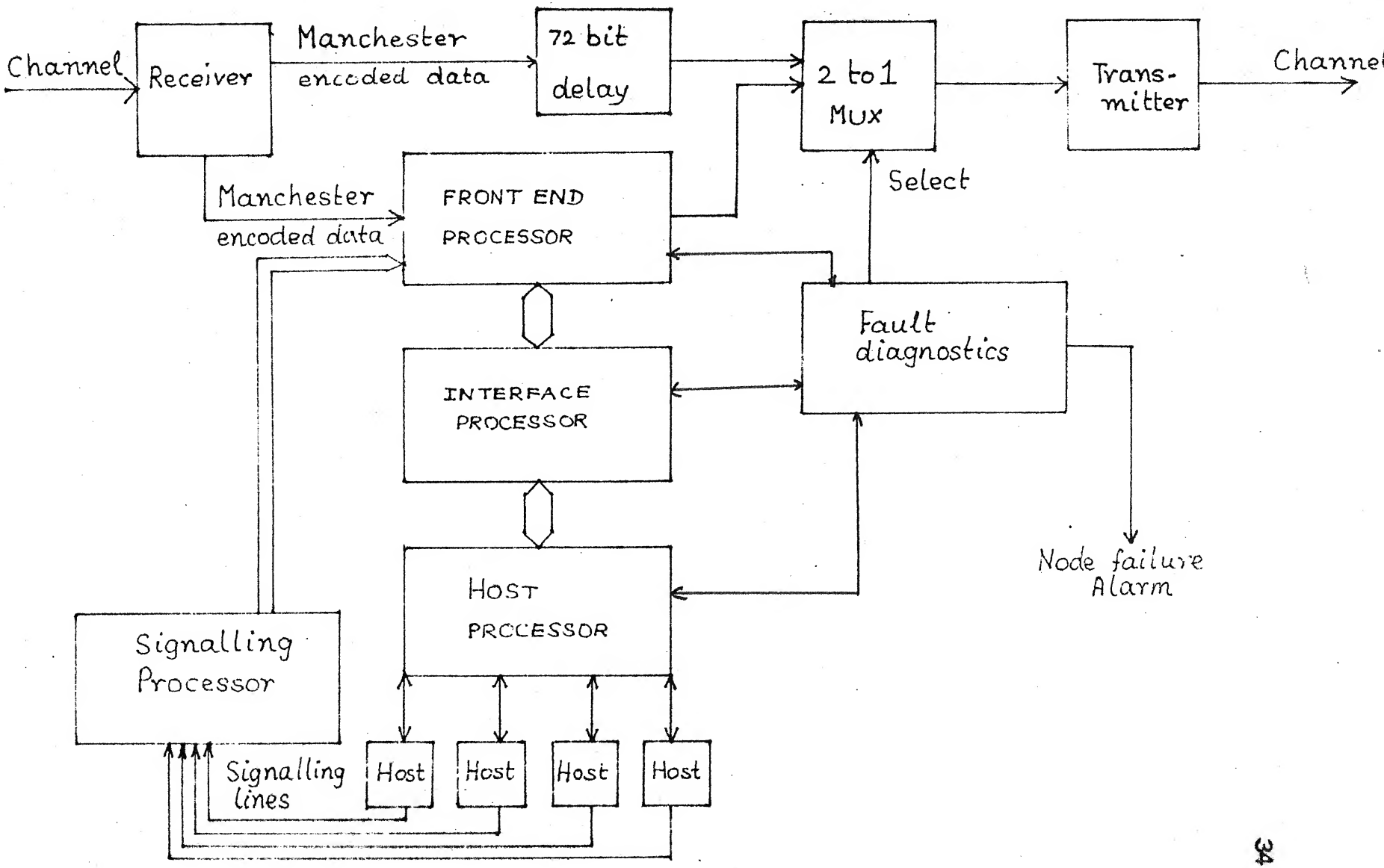


FIG. 3.4: BLOCK SCHEMATIC : NODE PROCESSOR

3.3.3 Functional Description: Node processor:

The Manchester-encoded data from the receiver is provided as input to the front end processor. This processor recovers the timing element, assigns and deassigns slots based on requests received and handles I/O processing with respect to the node. For this purpose it provides/ accepts signalling information through the signalling processor. The data is handed over to and received from the host processor (through the interface processor) frame to frame. The architecture of the host and interface processors are independent of the architecture of the front end processor.

The fault diagnostics unit maintains a check on the various elements of the node. In case of failure by the node the received data is transmitted unaltered. This is achieved by transmitting the received data after a 72 bit delay which has been incorporated to meet the timing requirements.

3.4 CONCLUSION:

This chapter outlined the design of a digital network for a local area environment suitable for voice and data. The front end processor was chosen for implementation in a 16 slot per frame format. The hardware implementation is discussed in Chapters 4 and 5.

CHAPTER 4

TIMING RECOVERY AND BIT SYNCHRONIZATION

In this chapter two aspects of the front end processor implemented-symbol timing recovery (STR) and frame synchronisation (FS)- are discussed. The former (STR) is necessary to achieve bit decoding and synchronisation. The latter (FS) is achieved by recognising a preset pattern which signifies the start of a new frame. With the help of these two parameters the received data is partitioned into the time slots to help in processing the same. These two aspects are discussed in the same order in the succeeding paragraphs.

4.1 SYMBOL TIMING RECOVERY (STR):

It was seen in the last chapter (Sec.3.2.7) that the transmitted data is Manchester encoded. The power spectral density of Manchester encoded data is shown in Fig. 3.2 . The spectrum indicates that the spectral line at the data rate is not unambiguous. Thus some kind of non-linear processing is necessary to generate the spectral line at the data rate. Digital gates offer one such possibility. The advantage lies in the fact that they are inexpensive and easy to implement.

4.1.1 Principle:

The STR technique implemented uses an Exclusive-OR gate to process a TTL compatible signal with a delayed replica of itself. The output of the Exclusive-OR gate is fed to a phase locked loop (PLL) centred at the data rate (Fig. 4.1). A detailed mathematical analysis of the same is available in [19]. The spectrum of the output indicates a non-ambiguous spectral line at the data rate. An alternative scheme makes use of the clock information available in the Manchester encoded data [20].

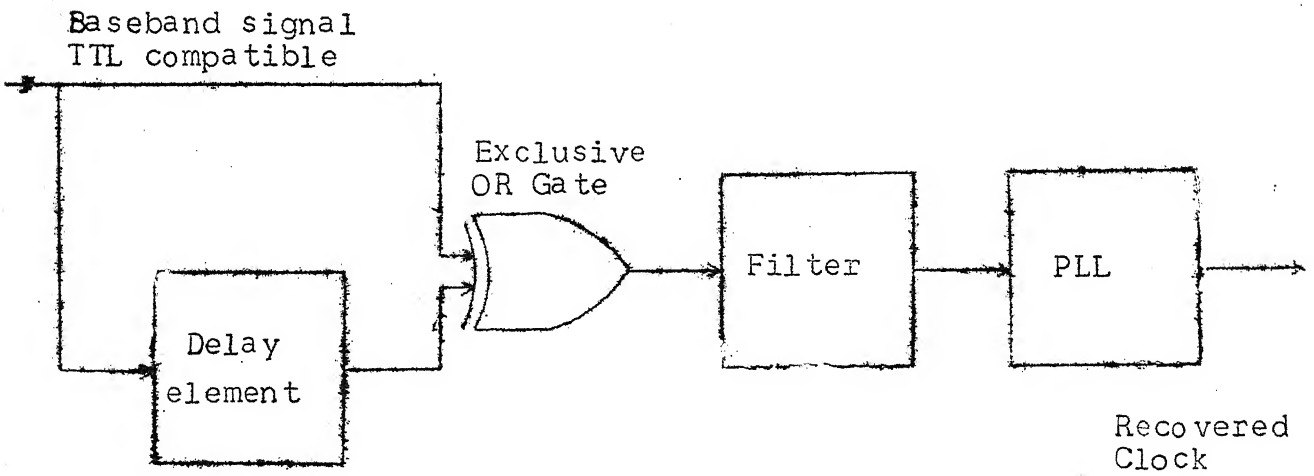


Fig. 4.1: STR circuit using digital processing elements and a PLL [4].

4.1.2 Clock Recovery Circuit: (Refer circuit diagram Appx B).

The serial data input (IC) is delayed by four inverters (IC 11-1/2, 3/4, 5/6, 9/8) in cascade. The Exclusive-OR gate compares the signal (IC 12/1] with its delayed replica (IC 11/8 - IC 12/2). The output (IC 12/3) is passed through an RC network. The amplitude reduced signal is fed to the input (IC 13/4) of the PLL (XR-215) through a coupling capacitor. The PLL has a nominal free running frequency equal to the data rate (1 MHz). The biasing components are as per recommendations from the manufacturer [21]. The synchronised clock output (IC 13/15) is capacitor-coupled to the input (IC 14/3) of a comparator (NE 529). The TTL compatible output (IC 14/11) is buffered by an inverter (IC 27). To increase fan-out the inputs (IC 27/1,5) and outputs (IC 27/2,6) are tied. The clock and inverted clock signals are provided to the system through the edge connector (JJ and JK). The PLL has an equivalent low pass BW of

4.1.3 Data Synchronisation:

The Manchester encoded data is presented at the input (IC 26/2) of a latch (IC 7474). The data derived clock (IC 27/2) is presented as the second input (IC 26/3). The synchronised data is available to the system through the edge connector (JF).

4.1.4 Frame Synchronisation:

The synchronised data (IC 26/5) is delayed using two AND gates (IC 25- 1,2,3 and 4,5,6). The delayed data (IC 25/6) is fed to two synchronous counters (IC 21/1,7,10,9, IC 22/1,9). The frame synchronisation pattern (Fig.) is detected by the counters and the NAND gate (IC 23/8).

4.2 BIT, SLOT AND FRAME COUNTERS:

4.2.1 Two Four Bit Synchronous binary counters (IC 31,32) and a NAND gate (IC 33) is used to implement a divide-by-36 counter. The reset signal (IC 33/6) is ANDed (IC 33/6 - IC 34/2, IC 23/8 - IC 34/1) with frame sync to ensure proper synchronisation.

4.2.2 A four bit synchronous binary counter (IC 35) is used to implement a divide by 16 counter. The bit counter reset pulse (IC 34/3) is inverted (IC 27/11-10) and connected as ripple carry inputs (IC 35/7,10). The frame synchronisation pulse is used as a master reset to synchronise counting (IC 35/1).

4.2.3 A four bit synchronous binary counter (IC 36) is used as a frame counter. The least significant bit of this counter (IC 36/14) is used as a memory select signal (JY) for the front end processor.

4.3 SYSTEM WRITE PULSE GENERATOR:

A write pulse generator formed by (IC 24) a monostable multivibrator (IC 74121), a resistor (5.1K) and a capacitor (150 pF) is used to provide a write pulse to the entire system (JL). The pulse has a width of 600 ns. The write pulse is synchronised with clock.

4.4 CONCLUSION:

To summarise, the clock recovery circuit (Appx B) provides the following to the system :

a) Timing recovery and bit synchronisation

b) System clock

c) Bit slot and frame counters

d) Write pulse

With the help of this information the input output processing is carried out. The process is described in Chapter 5.

CHAPTER 5

THE NODE FRONT-END PROCESSOR

In this chapter the implementation of the node front-end processor is considered. This processor assigns and deassigns slots on demand and processes the serial input data stream. The processor hardware is divided into 8 major blocks. These are as under:

a) Timing recovery circuit - Discussed in Chapter 4.

b) Serial-in Parallel-out circuit - discussed in Section 5.1.

c) System control circuit - discussed in Section 5.2.

d) Address directory circuit - discussed in Section 5.3.

e) Multiplexed memory circuit - discussed in Section 5.4.

f) Main system memory circuit - discussed in Section 5.5.

g) Port status register circuit - discussed in Sec.5.6.

h) Parallel-in serial-out circuit- discussed in Sec.5.7.

The schematics/circuit diagrams are attached at appendices B to G3. The system control lines status and functions performed are described in Table 5.1 to 5.4. Appendix A describes the conventions followed in the

schematics in relation to the actual circuits.

5.1 SERIAL-IN-PARALLEL-OUT (SIPO) CIRCUIT:

The circuit (Appendix C) essentially consists of two sets of shift registers (IC 13-17, 31-35), two-to-one multiplexers (IC 22-2A), a decoder (IC 21) and gating circuitry (IC 11,12) for generating clock and output select controls. The shift register sets (IC 13-17 , 31-35) are connected in cascade to form 40-bit shift register banks. The tri-state two-to-one multiplexers (IC 22-2A) select one bank of shift registers for output. The outputs of the multiplexers are appropriately configured to form a 8-bit system data bus. The bytes are chosen by the decoder (IC 21) with the help of the system controls (Table 5.1) E_3 - E_5. The header information of slot (n-1) available in the shift register (IC 17/IC 35) is extracted through a multiplexer (IC-43). Called party address (assuming it to be present) is similarly extracted (IC 41 and 42).

5.2 SYSTEM CONTROL CIRCUIT:

The schematic of the circuit is placed at Appendix D. The control bus is divided into 3 groups.

i) Address directory controls - EPROM lines E_0-E_2
ii) Input/output controls - EPROM lines E_3-E_5
iii) Port status controls - EPROM lines E_6-E_7.

The control circuitry consists of 5 stages

- Generation of strobe and output enable signals for the latches (IC 11,12)
- the EPROM (IC 15)
- the output latches (IC 13,14)
- address directory RAM address generator (IC 21)
- Device select logic generator for multiplexed memory (IC 31).

The state of control lines and their interpretations are placed in Tables 5.1 to 5.4. The control states are modified by the header received, suitably.

5.2.1 Control Generation:

The LSB of bit counter (IC 11/1) and its complement (IC 11/2) are gated with clock (IC 12/2,5) to produce two strobe signals (IC 12/3,6). The LSB of the bit counter and its complement are used to enable the latches (IC 13,14). The outputs of the latches are bussed. The input to the latches is obtained from the EPROM (IC 15). The bit counter outputs constitute the address bus of the EPROM whose outputs are permanently enabled.

5.2.2 RAM Address Generator:

This accepts the slot counter outputs (slot n) as inputs, decrements it by 1 and outputs the result (slot n-1).

Table 5.1: SIPO CIRCUIT CONTROLS

Clock state	EPROM Control E_5	E_4	E_3	Decoded output	Result	Action with respect to memory
00-07	0	0	0	$\bar{0}$	No action in this card	-
0C	0	0	1	$\bar{1}$	Byte 5 placed on system data bus (SDB)	Memory write (MW)
0B	0	1	0	$\bar{2}$	Byte 4 placed on SDB	MW
0A	0	1	1	$\bar{3}$	Byte 3 placed on SDB	MW
09	1	0	0	$\bar{4}$	Byte 2 placed on SDB	MW
08	1	0	1	$\bar{5}$	Byte 1 placed on SDB. Contains information for interface/host processor.	MW
-	1	1	0	$\bar{6}$	No action in this card	-
-	1	1	1	$\bar{7}$	No action in this card.	-

Table 5.2: PISO CIRCUIT CONTROLS (PROPOSED)

Clock State	EPROM Control E_5	E_4	E_3	Decoded output	Result	Action with respect to memory
-	0	0	0	$\bar{0}$	No action in this card	-
14	0	0	1	$\bar{1}$	Byte 5 placed on SDB	Memory read (MR)
13	0	1	0	$\bar{2}$	Byte 4 placed on SDB	MR
12	0	1	1	$\bar{3}$	Byte 3 placed on SDB	MR
11	1	0	0	$\bar{4}$	Byte 2 placed on SDB	MR
10	1	0	1	$\bar{5}$	Byte 1 placed on SDB. Contains header information	MR
-	1	1	0	$\bar{6}$	No action in this card	-
-	1	1	1	$\bar{7}$	No action in this card	-

Table 5.3: PORT STATUS REGISTER CONTROLS (PROPOSED)

Clock state	Header	EPROM Control E_8	E_7	Decoded output	Result
00	XXX	0	0	$\bar{0}$	No action in this circuit
01	011	0	1	$\bar{1}$	Memory read.
02	011	1	0	$\bar{2}$	Memory write.
03-23	XXX	1	1	$\bar{3}$	Update port status by signalling processor

Table 5.4: ADDRESS DIRECTORY CIRCUIT CONTROLS

Clock State	EPROM Controls $\bar{E}_1$	$\bar{E}_2$	$\bar{E}_3$	Decoded output	Result
00	0	0	0	$\bar{0}$	No action in this circuit
02	1	0	0	$\bar{1}$	The address directory RAM (ADRAM) gets the contents of the I/O port.
01	0	1	0	$\bar{2}$	ADRAM memory location corresponding to slot counter (n-1) is cleared.
06	1	1	0	$\bar{3}$	ADRAM memory location corresponding to slot counter (n-1) is read.
03	0	0	1	$\bar{4}$	Generates strobe for latching called party address.
04	1	0	1	$\bar{5}$	Selected memory location gets called party address.
05	0	1	1	$\bar{6}$	The latch which selects the main memory/user MUX memory is cleared.
08-C, 10-14	1	1	1	$\bar{7}$	Address latch outputs are enabled and address placed on address bus

5.2.3 Device Select Logic:

The device select logic output (IC 31/6) goes low whenever a memory is selected for input/output processing. The inputs to this device are the control lines E_3, E_4 and E_5 (IC 31/1,2,4).

5.3 ADDRESS DIRECTORY CIRCUIT:

The circuit essentially consists of two stages

- The I/O Port card (Appendix E1)
- The RAM card (Appendix E2)

5.3.1 The I/O Port Card:

The circuit essentially consists of an I/O port (IC 13) and associated decoder (IC 11,12), control decoders (IC 15,16,25) and logic gates. An 8085 microprocessor system was assumed to be the signalling processor (Ref. Fig. 3.). The system (S_1, S_0, IO/$\overline{M}$, $\overline{WRITE}$) and address (A_7, A_6) lines are decoded (IC 11) and the result inverted (IC 12/5,6) to obtain a strobe to latch in data. The asynchronous request is synchronised with respect to the front-end by means of a latch (IC 14). The SR flip-flop output is returned as a flag to the signalling processor. The flag in its 'high' state permits data entry into the I/O port (IC 13). The synchronised request is inverted and returned

as a part of device select logic to the I/O port. The I/O port when selected places its contents on the data bus and simultaneously resets the SR flip-flop. The control decoders (IC 15,16,25) with associated logic gates generate the appropriate device select and read/write control signals as shown.

5.3.2 The RAM Card:

The memory block (IC 11,12) is configured as a 1K x 8 RAM. The address lines are obtained from the control card (as slot n-1); the data bus is connected to the latches (IC 21,22) and I/O port (Sec. 5.3.1 (IC 13)). The latches (IC 22,21) place $(00)_H$ and the called party address on the SDB respectively when selected. The output latch (IC 23) stores the content of the addressed memory location. The latch (IC34) stores information whether the address is valid or not. (All addresses other than $(00)_H$ are valid). This result is obtained by ORing the bus lines (IC 31,32). The result controls the strobe and output enable signals to the output latch (IC 23).

5.4 MULTIPLEXED MEMORY CIRCUIT:

This circuit (Appendix F) consists of two sets of memories (IC 14 and 15, IC 24 and 25) shared between two users. The memories are switched frame to frame. The

address and control lines use unidirectional two-to-one multiplexers (IC 11-13, 21-23). Multiplexing of bidirectional data lines is achieved by transceivers (IC 16-1A, 26-2A). The outputs of the transceivers (being tristate outputs) are configured as two buses - one towards the front end processor as a system data bus (SDB) and the other as a user interface bus. Logic gates (IC 16 and 26) derive the controls for the transceivers. The selection of memories for the front end is carried out by the LSB of frame counter (select line).

5.5 MAIN SYSTEM MEMORY CIRCUIT (PROPOSED):

The schematic at Appendix G1 describes one implementation of the main system memory. The capacity of the memory should be greater than the frame length. In the present case the memory capacity is 8N bytes where N is the number of slots per frame. This circuit has not been tested.

5.6 PORT STATUS REGISTER CIRCUIT (PROPOSED):

The port status register (Appendix G2) has been configured as part of a processor memory. The node front-end processor places a HOLD request catering for the worst case (maximum delay). On receipt of HOLD Acknowledge the front-end processor reads/carries out an update of the port status register (memory). The front-end processor relinquishes use of the buses on completion of access. This circuit has not been tested.

5.7 PARALLEL-IN SERIAL-OUT (PISO) CIRCUIT (PROPOSED):

The layout of the circuit (shown in Appendix G3) is quite similar to the layout described in Sec. 5.1 (Appendix C) for the SIPO circuit. This circuit, too, has not been tested.

A better method of integrating the circuits shown in Appendices C, G1 and G3 is discussed in Section 7.2.

5.8 CONCLUSION:

In this chapter the implementation of a dedicated front-end processor of a node was discussed. The design is modular and needs only minimum information from the subscribers. The applications and expected performance is discussed in the next chapter.

CHAPTER 6

EXPECTED PERFORMANCE OF NETWORK AND UTILISATION

The design of a network for integrated services and the realisation of the front end processor of a node have been discussed so far. In this chapter the parameters of interest - efficiency/throughput and call set up and disconnect times are discussed.

6.1 CALL SET UP TIME:

6.1.1 Assumptions:

i) A call is considered originated when the called party address has been transmitted to the host processor.

ii) The same processor performs the jobs of interface and host processors (Fig. 3.4)

iii) The signalling processor (Fig. 3.4) (processor which handles signalling information from and to the host) is different from the host/interface processor.

iv) The called party is assumed to respond in T secs.

6.1.2 Calculation:

Let the signalling processor forward the call request to the front end processor. This is assumed to take place in frame F. Assuming a free slot in this frame the signalling information is transmitted in frame F+1. The called node receives this frame in the same frame time, processes it and places it in the user multiplexed memory. The interface/host processor of the called party receives this informationin frame F+2 and extends signalling information to the called subscriber (for example a microprocessor). Let the called subscriber respond in T secs. In the return path the acceptance information is transmitted in frame $(F + 2 + \frac{T}{.5ms})$ where $(\frac{T}{.5ms})$ is an integer. (If $\frac{T}{.5ms}$ is a fraction it is rounded off to the next highest integer). This reaches the calling party node during the same frame interval. The acceptance information is conveyed to the host processor in frame $(F + 3 + \frac{T}{.5ms})$. The virtual path now may be considered as having been set up between the calling and called subscribers.

In the case of telephony, the response time of the called subscriber is generally large in comparison to the time taken by the network to transmit/receive such signals. In the case of data users it is reasonable to expect that

the called party response time (T) is of the order of a millisecond;for example, a microprocessor can be a called party. Thus one can expect a call set up time of the order of 5 milliseconds which is adequate for a fast circuit switched approach (sec. 2.1.2(b)).

6.1.3 Slot Reassignment Delay:

A subscriber may be considered to have relinquished a slot immediately after his last transmission. This information is available when the slot assigned to the subscriber is deassigned in the next frame. Further the slot has to travel to the next node before it is re-assigned. Thus this delay could be considered to be of the order of one ms.

6.2 APPLICATIONS:

The call set up and disconnect times are of interest in the case of interactive data users whose average message length is 1000 bits , with a 'think' (idle) time of 10 seconds or so [3]. The efficiency, in such a case, may be defined as under:

$$\text{Efficiency} = \frac{\text{Time taken to transmit data}}{\text{Total time circuit is used}}$$

The channel supports 64 Kbps; hence the time taken to transmit 1000 bits is approximately 16 ms. The time for which/the

circuit is used is the sum of call set up and relinquish times and time required to transfer data. This is 22 ms. Thus the efficiency for the present case is approximately 70%. The circuit, thus, meets the qualifications prescribed for a fast circuit switched approach for data (Sec. 2.1.2(b)).

6.3 CAPACITY UTILISATION:

The maximum capacity (when all available slots are used) that can be utilised is given by the formula

$$\text{Capacity utilisation} = \frac{(N-1)\times 32}{N\times 36} \qquad (6.1)$$

where N is the number of slots/frame. For the present case implemented (16 slots/frame) the capacity utilisation is 83.3%. It is seen that this value increases with increasing N and asymptotically reaches a value of 88.8%.

6.4 THROUGHPUT:

If n be the number of slots used in a frame then the throughput is given by the expression

$$\text{Throughput} = \frac{n \times 32}{N \times 36} \quad \text{for } 0 \leq n < N \qquad (6.2)$$

The above equation indicates that the throughput increases linearly with input till n = N-1 (when saturation occurs).

6.5 SOME SPECIAL PROPERTIES:

As the NW can support any mix of voice and data it is

expected that its performance, in terms of throughput, is likely to be superior to the conventional NWs. Further the delay performance (time taken for transmitted information to reach the called party) is expected to remain unaffected by the load on the NW (as in the conventional circuit switched approach). The network can be suitably modified for a hybrid switched approach easily. Network topology has removed the need for a routing algorithm which helps to reduce overheads.

CHAPTER 7

CONCLUSIONS

7.1 CONCLUSIONS:

The design of a 7.2 Mbps 100 slot/frame system and the implementation of a scaled down version has been discussed in the earlier chapters. The architecture of the NW and its processing power should be adequate to meet the needs of voice and data users in a local area environment. The virtual circuits meet the CCITT recommendations of a traffic channel in the ISDN environment. However some modifications can be carried out to the present work to improve its performance/complete the NW.

7.2 MODIFICATIONS:

i) The serial-in parallel-out and parallel-in serial-out circuits along with the main memory may be replaced by one single card containing universal shift registers (say 74199). The suggested architecture is shown in Appendix H Such an architecture reduces the number of ICs used.

ii) Low power devices such as CMOS or high speed CMOS devices could be used to reduce the power consumption.

iii) A star architecture of the host processor with an independent memory for each user/group of users would reduce the response time of the subscribers.

iv) Faster RAM's may be used with better bidirectional bus buffers such as 74LS 245.

v) The course of action followed in a slot could be based on the header information i.e., an interrupt driven architecture. This would increase the bus idle time for system diagnostics.

7.3 SUGGESTIONS FOR FUTURE WORK:

i) The host and interface processors should be designed.

ii) A loop controller capable of interfacing a larger NW needs to be designed. The loop monitor in addition could assist in data retrieval and act as a message dump (mail box) for users.

ii) Fault diagnostics and node bypass circuitry for the system needs to be designed.

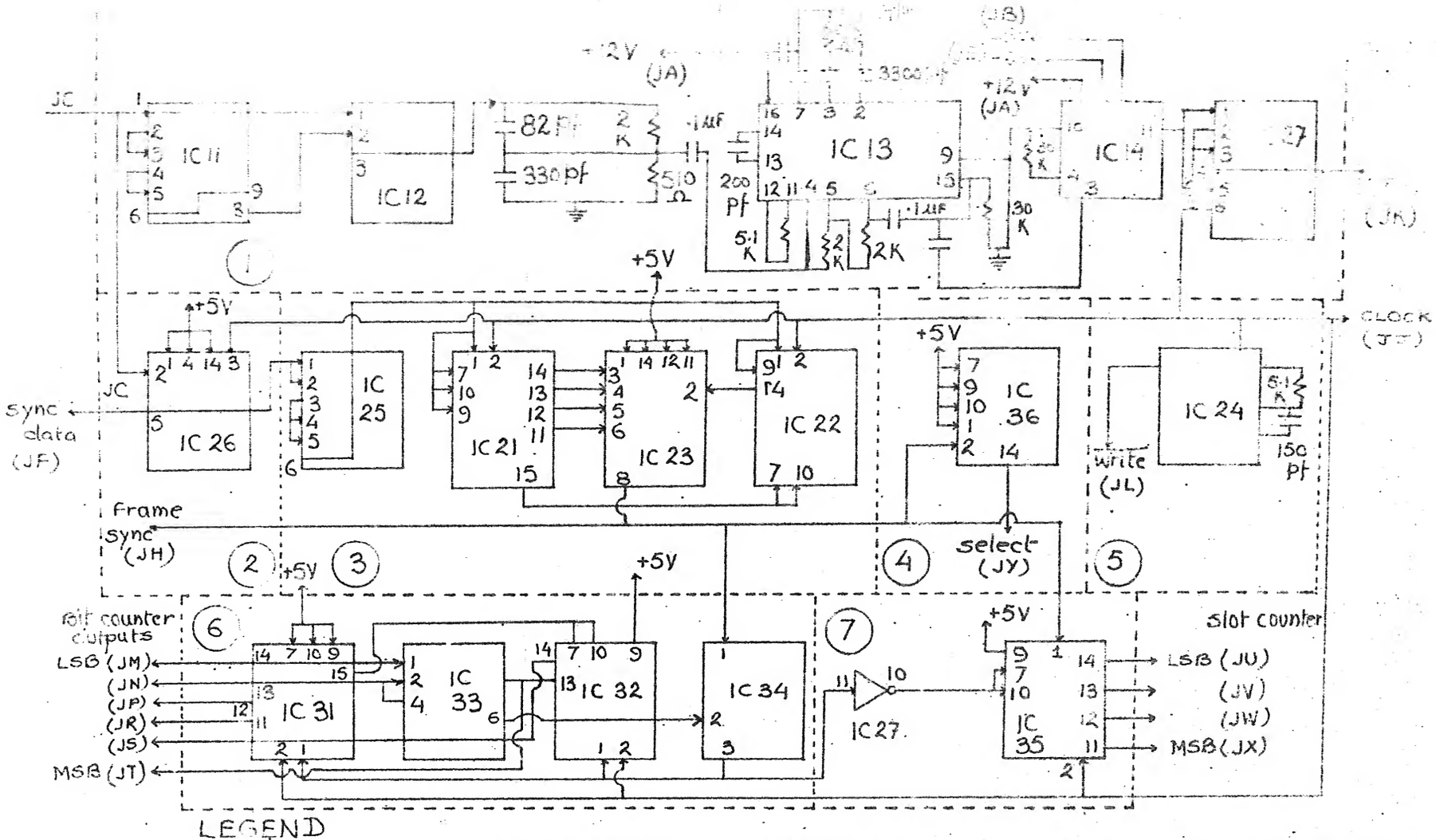
iv) Based on the completed network, traffic patterns could be studied with a view to optimise selected parameters (cost, distribution of of voice and data users in a node, average wait time of a subscriber for a call request to materialise etc.) and evolve a better network.

APPENDIX A

NOTES ON CONVENTIONS ADOPTED IN CIRCUIT DIAGRAMS

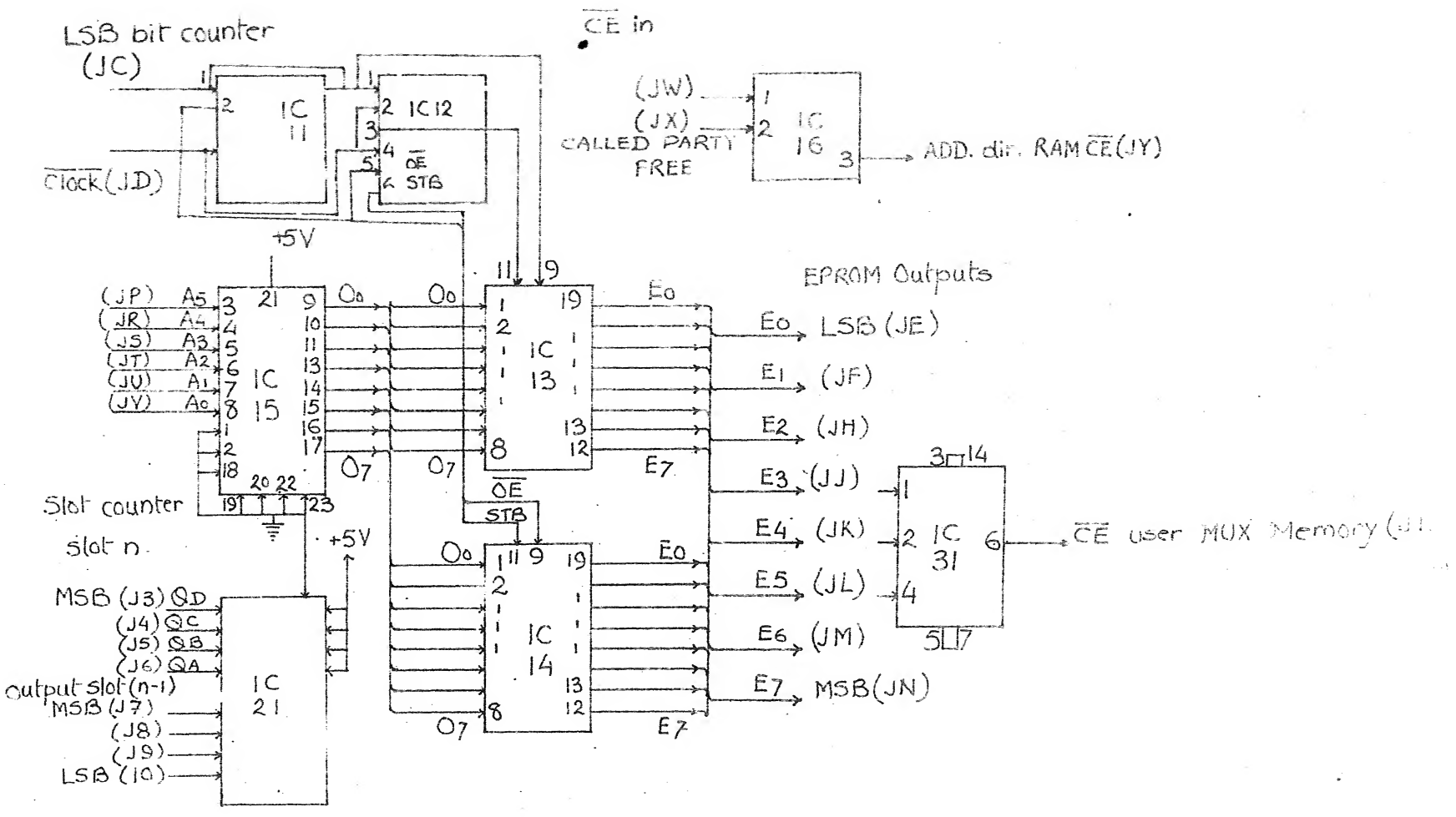
The conventions followed in representing the actual circuit is listed below.

1. All components are placed on the top of the card.
2. The edge connector is placed to the left of the card.
3. The edge connector pins are numbered from J1 to J22 for the top layer and JA to JZ (except JG, JI, JO and JQ) for the bottom layers.
4. An IC number consists of 2 alphanumerics. The first number refers to the row number and the second to the column number. The column numbers are in hexadecimal.
5. ICs are numbered from left to right and top to bottom.



1	CLOCK RECOVERY	3.	FRAME SYNC	5.	WRITE PULSE	7.	SLOT COUNTER
IC 11	IC 7404	IC 25	IC 7408	IC 24	IC 74121		
IC 12	IC 7486	IC 21	IC 74163			IC 35	IC 74163
IC 13	IC XR-215	IC 22	IC 74163	6	10BIT COUNTER		
IC 14	IC NE 529	IC 23	IC 7430	IC 31	IC 74163		
IC 27	IC 7404			IC 32	IC 74163		
		4	FRAME SELECT	IC 33	IC 7420		
2	DATA RECOVERY	IC 36	IC 74163	IC 34	IC 7408		
IC 26	IC 7474						

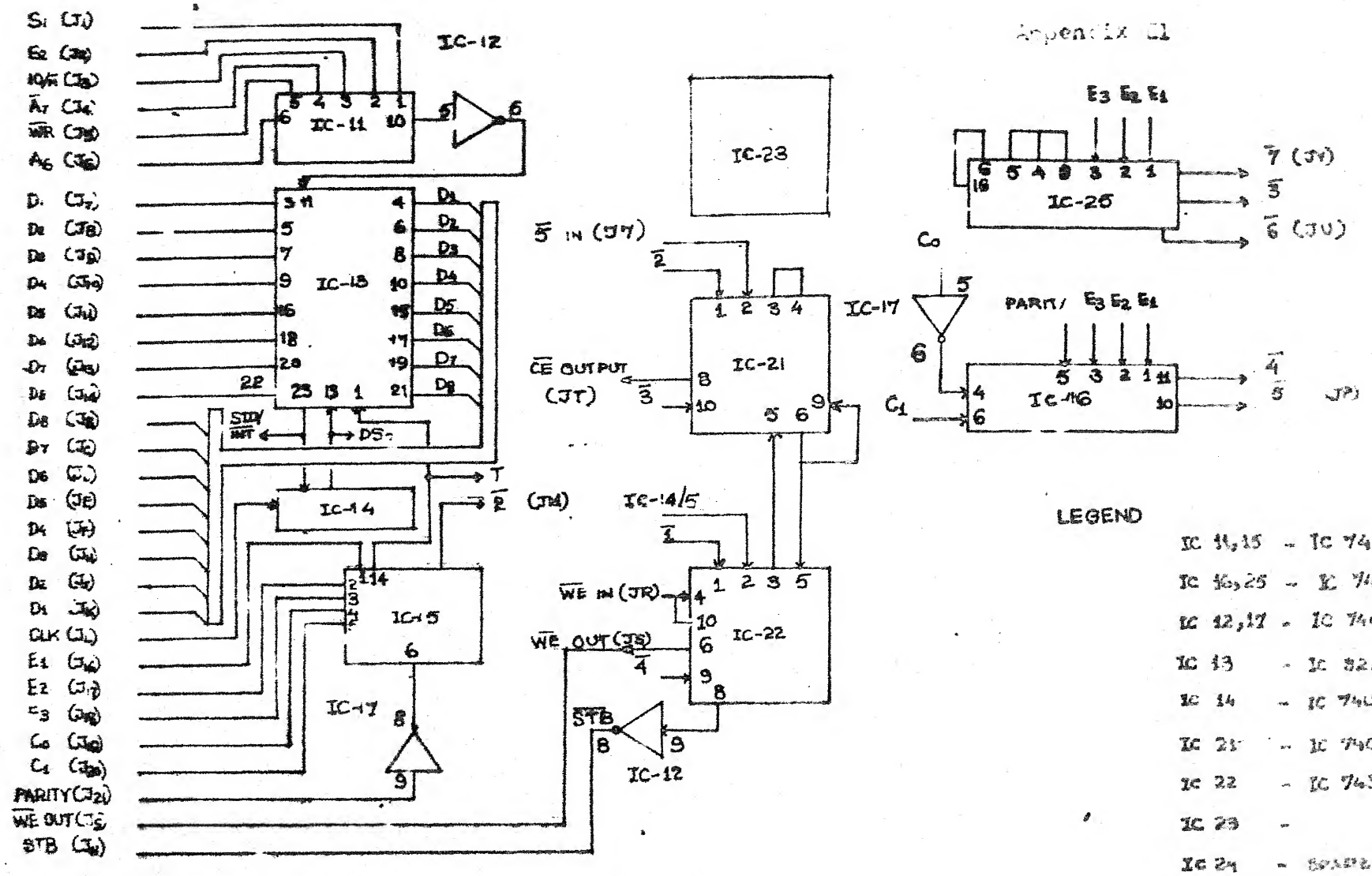
TIMING RECOVERY CIRCUIT



LEGEND.

IC 11	IC 7404	IC 15	IC 2716
IC 12	IC 7408	IC 16	IC 7432
IC 13	IC 8282	IC 21	IC 7483
IC 14	IC 8282	IC 31	IC 7425

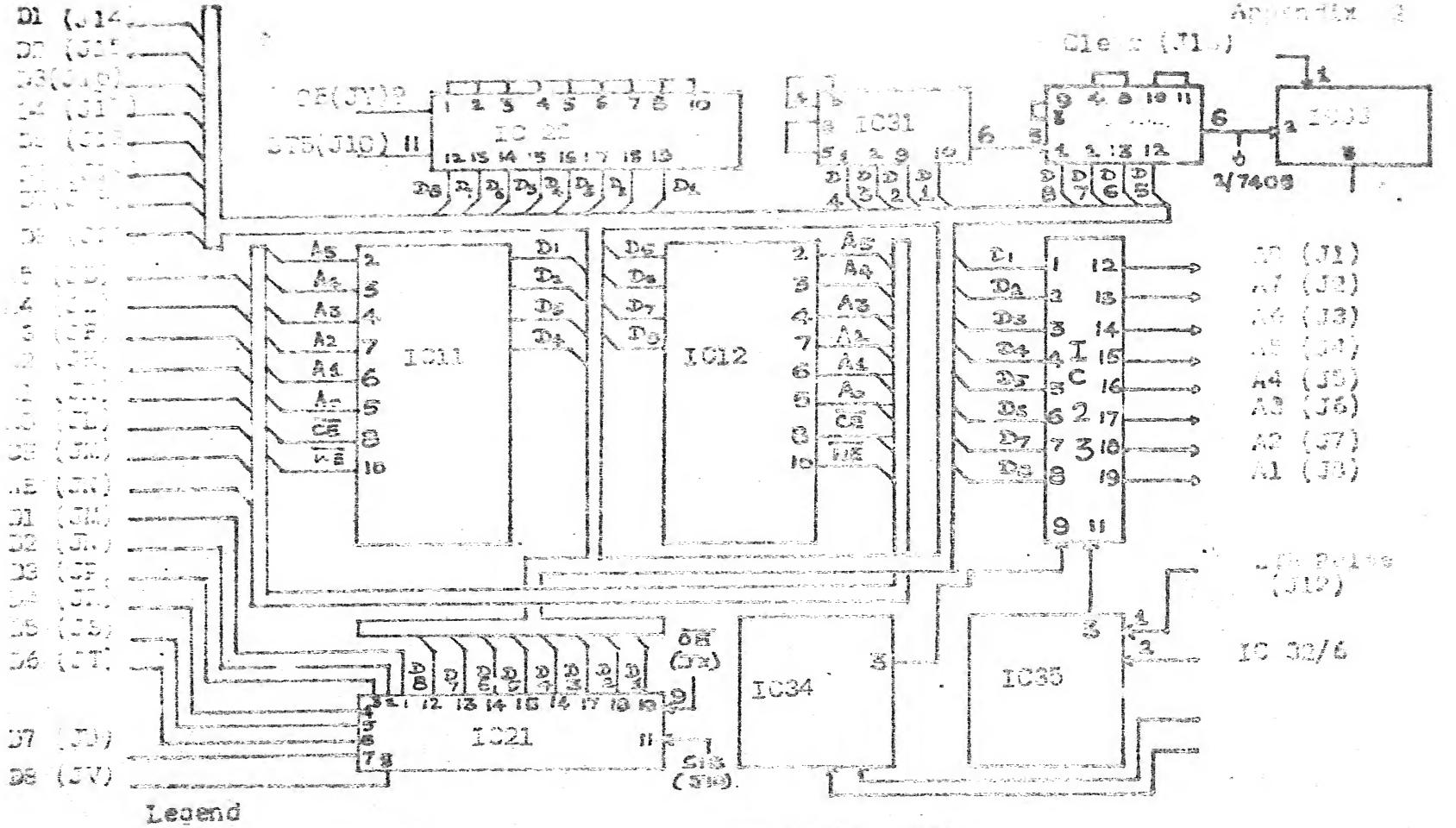
Control circuit for front end processor.



Address Directory Circuit: I/O Port Card

LEGEND

IC 11,15 - IC 74LS138
IC 16,26 - IC 74LS139
IC 12,17 - IC 7404
IC 13 - IC 8212
IC 14 - IC 74LS374
IC 21 - IC 7408
IC 22 - IC 7432
IC 23 -
IC 24 - 8255

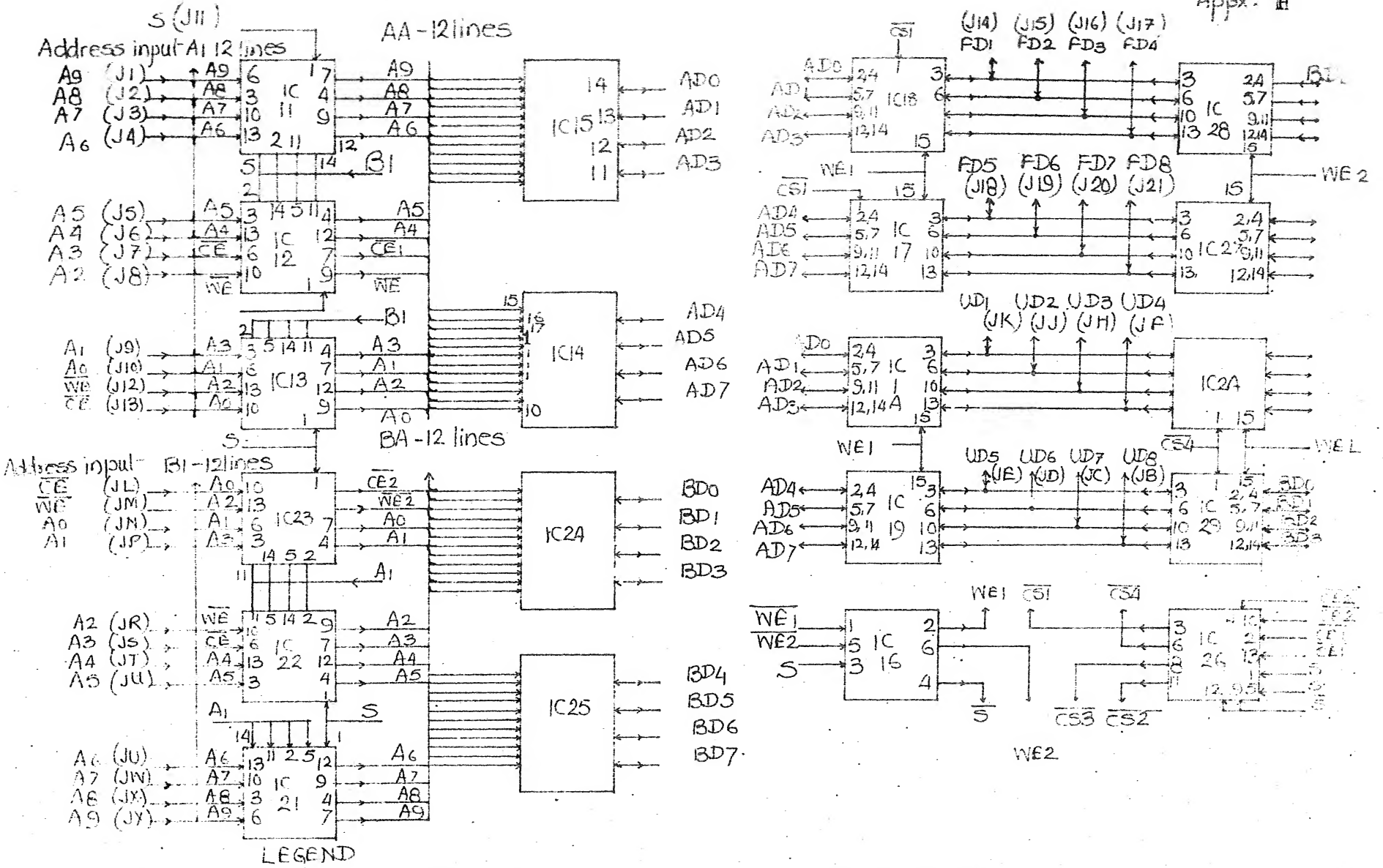


1. Memories
   IC 11,12 - IC 2114

2. Octal latches
   IC 21,22,23 - IC 8282

3. Logic Gates
   IC 31,32,34 - IC 7432
   IC 35 - IC 7403

4. Latch
   IC 34, - IC 74LS74.

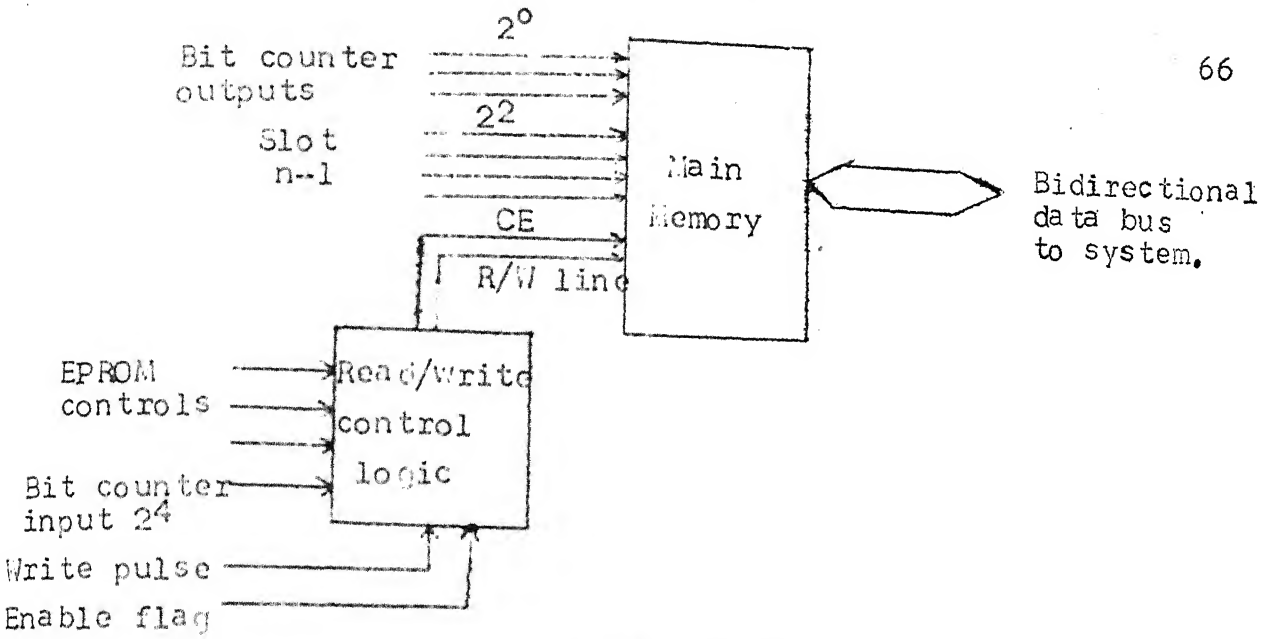


1. Multiplexers;
   IC 11-13, 21-23 - IC 74S257
2. Memories
   IC 14, 15, 24, 25 - IC 2114
3. Transceivers
   IC 17-1A, 27-2A - IC 8216
4. Logic
   IC 16 - IC 7404
   IC 26 - IC 7432

NOTE: All labels bearing same name are interconnected

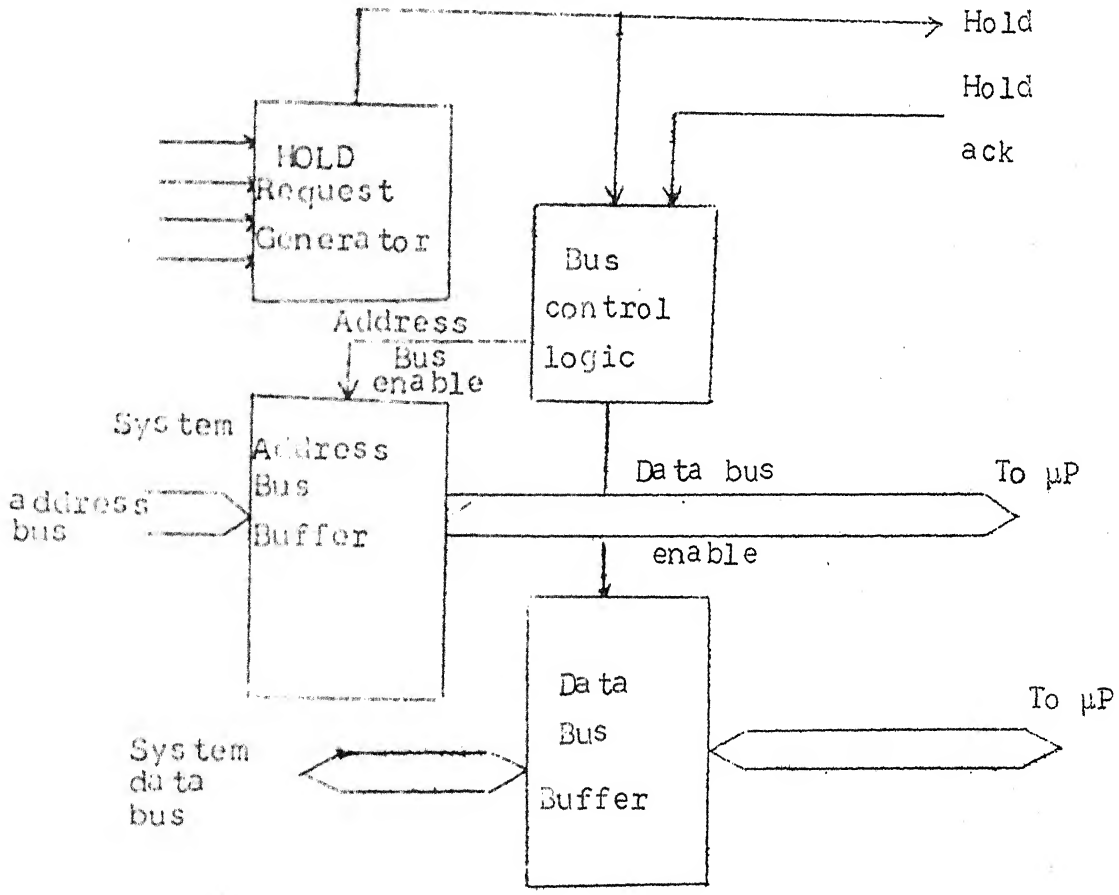
Multiplexed Memory circuit

Appendix G1

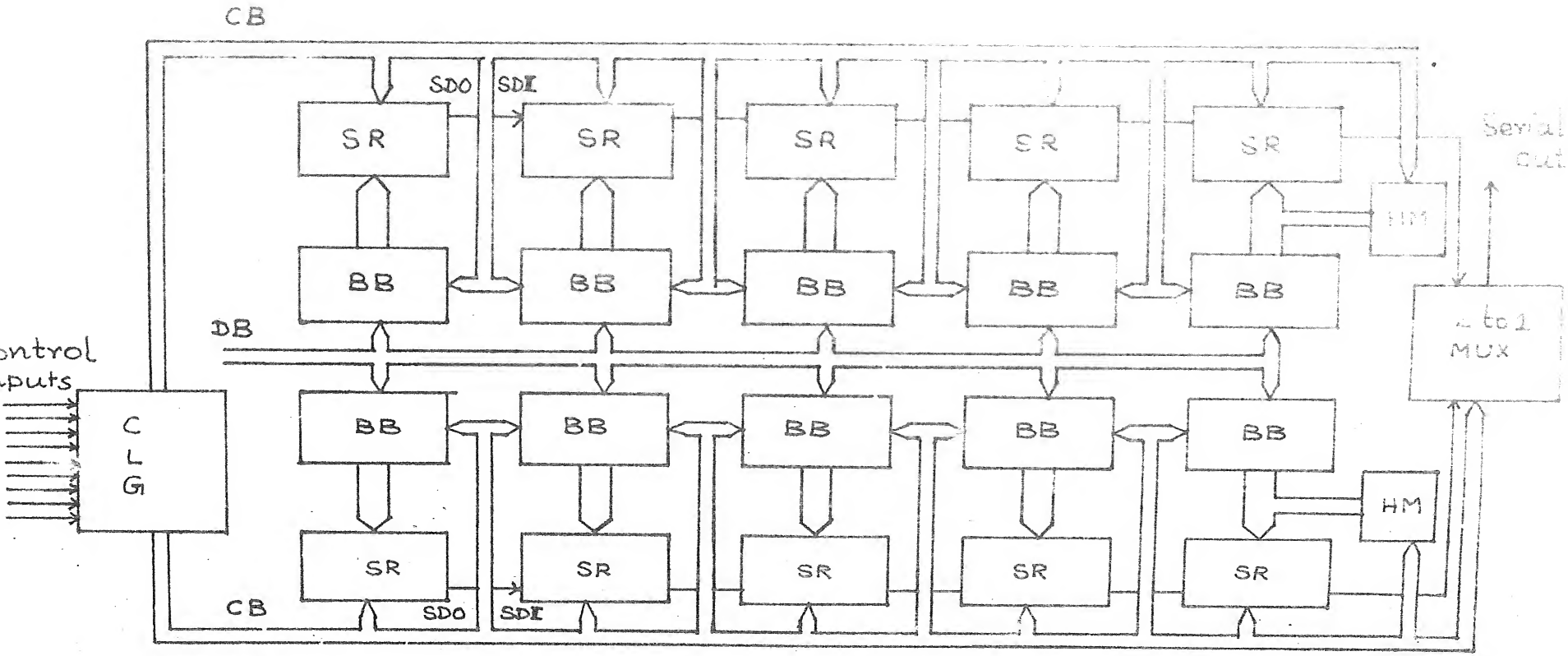


Main system memory

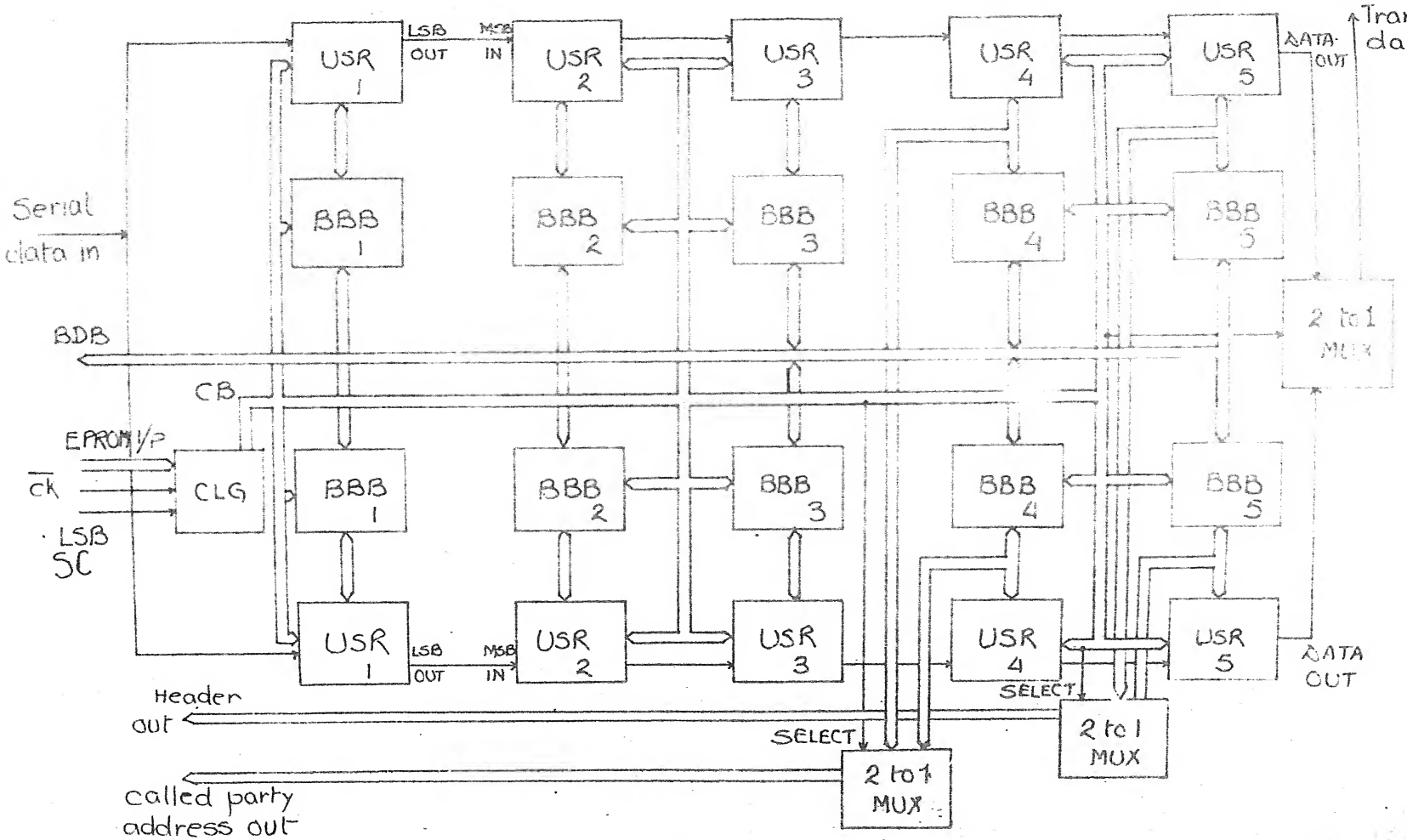
Appendix G2



Port Status Register



BLOCK SCHEMATIC : PARALLEL IN SERIAL OUT CIRCUIT



LEGEND:

USR : Universal shift register.
BBB : Bidirectional Bus buffer.
BDB : Bidirectional data bus
CB : Control bus
CLG : Control logic generator.
LSB-SC : LSB slot counter

Front end I/O card.

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